A Systems View of Test and DFT

Outline

System and Board Test Issues
- Illustration of a system - functional and structural hierarchies and O&M
- Production test
- Test and diagnosis in the field
- Repair test

Test and DFT for SoC
- SoC characteristics
- State-of-the-art Test and DFT for SoC
- Optimal DFT implementation for different structures
- Access and isolation
- Chip level integration and external access
- Design flow
A Systems View of Test and DFT

System and Board Test Issues
Radio Network - Traffic View

O&M - Network Element Management

Centralized
E.g Remote SW handling, Network Product Inventory, Planned Area implementation

OMC
OMC

RANOS

Coordinated handling of multiple NEs

Embedded Element Management

TCP/IP over ATM

Each node contains all its own O&M functionality for EM.

Centralized
E.g Remote SW handling, Network Product Inventory, Planned Area implementation

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Embedded Element Management

Each node contains all its own O&M functionality for EM.
RBS cabinet

Capacitor Unit

Base Band Subrack

MXRX: RX Module with RX Filters
TX/RX: Transmitter/Receiver Board
ENRC: Enriched RX Board
RDAC: Radio Access Board
SN: Switch Control Board
TM: Time Module Board
TX: Transmitter Board
RX: Receiver Board
AL: Alarm Interface Board
TXRX: Transmit/Receive Board
AP: Access Power Board
ANT: Antenna Interface Unit
TNC: Transceiver Board
RF: Radio Frequency Interface Board
IRU: I/O Radio Unit Board
SCD: Switch Control Board
B: Base Band Subrack
AG: Adjunct Board
MPA: Multi-Channel Power Amplifier
RF Subrack

Figure 6

Capacitor Unit
RBS Control and Communication
Subrack Space Switching

- Multi-purpose cell switch
  - Traffic
  - SW Loading
  - Internal Control Paths (ICPs)
- QoS separation
- Switch sub-components
  - Space Switch Interface Circuit (SPIC)
  - ATM Switch Core Circuit (ASCC)
- 1 + 1 switch redundancy
- Explicit routing - stateless HW
- Non-blocking within subrack
  - 510 Mbps SPIC - SPIC
  - Subrack capacity 28 × 510 Mbps
  - ASCC made for 28 × 622 Mbps
  - 53-byte cell size
RBS Control Structure
Physical building blocks of the RBS

To/from RNC (traffic & O&M access)
- Mains Power
- To/from TMS antenna'
- O&M access, TC
- SiteLAN
- EACU
- External alarms
- SCB
- TX
- RX
- BBIF
- TMS
- MP
- EACU
- O&M access, TC
- SiteLAN
- External alarms
- Mains Power
- RBS cabinet
- Power subrack
- CU or PSU/PCU
- Baseband subrack
- ET
- TU
- RFIF
- TRX
- AIU
- MCPA subrack
- MCPA
- TMA+RET
- Or RET

Mains Power
To/from RNC (traffic & O&M access)
Micro RBS
Board - Technology

• General observation: boards are very heterogeneous
• 16 layer fine pitch
• SMT, often 0.5 mm pitch packages
• BGA, CSP, DCA introduced, integrated discretes
• Mix of single ended and differential signals, e.g. LVDS, 10-200 MHz usual, +600 MHz sometimes
• On-board uP, as std components and/or in ASIC
• DSPs common in some products
• Often few, very large ASICs/SoCs
Board - Technology cont.

• FPGA common when introducing new concepts, else ASIC/SoC are deployed for major functionality
• Except the above and bus drivers, other std digital components are rare
• Oscillators and power supply
• HS electrical and opto interfaces
• Sometimes protection against over-voltage, short-circuit, etc.
ET Board
Board - Test and DFT

- Mix of many methods, more process oriented now
- Vision and X-ray, ICT
- Focus on testing interconnects and type and placement of components
- Incoming inspection rare
- Boundary scan whenever possible
Board - Test and DFT cont.

- Functional test common in radio and fixed access
- P-BIST used for functional test at speed, e.g. testing memories, interface loops
- Special instruments used in some cases, e.g. when testing communication protocols
Board - Test Problems

- Test mainly static, many dynamic faults not detected
- Functional test, e.g. P-BIST has poor diagnostics
- Download of test SW, FPGA etc. is slow
Board - Technology Forecast

- Feature sizes decreasing, convergence towards MCM
- Improved yield
- Micro BGA, CSP, DCA common
- Integrated discretes
- Few standard components
- HS interconnects dominating, e.g. LVDS
- Going towards single board systems
Board - Test Requirements

- Statistical based process test after production ramp-up
- Support for easy test of internal and external interfaces
Sub-rack - Technology

- Often multidrop, std backplane
- HS serial busses, LVDS
- Often control and data over same bus
- Un-structured multi-wire interconnects are rare
Sub-rack - Test and DFT

- Objective: to find functional anomalies and low level HW faults
- Done mainly by system level test SW
- Functional test at system speed
- Mock-up of system environment
- Simulated operator interface common
- Standardized system test platform also usual
- Test often during long time and elevated temperature
Sub-rack - Test Problems

- Diagnosis extremely time consuming
- Often trial-and-error
- Boards returned to board test are often NFFs
Network Node - Technology

• Often single or few cabinets or “box”
• Communication via fiber, microwave or radio
• Techniques for robustness and fault tolerance varies
• Network management via IP with web MMI
Network Node - Test and DFT

• Complete node test now introduced
• Replaces much of installation test
• Checks that user configuration of HW and SW works as specified
Sub-rack/Node - Test Requirements

• Inter-board interconnect test, dynamic and static better supported
• More HW test support in general
• DFT functions easily controlled by system level SW
• Hierarchical access to lower level DFT
Supervision

• Dependability is becoming a major competitive characteristic
• Soft errors and shorter IC life span
• Better and more structured supervision needed
• Both on-line and off-line test required
Test and Diagnosis in the Field

• Alarm driven tests:
  • Judge severity
  • Stop fault propagation (block function, etc.)
  • Redirect traffic
  • Test (and diagnose to plug-in unit)
  • Restart or (replace faulty unit and restart)
• Preventive tests: performed regularly and/or at low load
• Critical factors:
  • Detection capability
  • Diagnostic accuracy
  • Preventive tests: test time
Repair Test

- Always performed at plug-in units (mostly boards)
- Legacy testers and test programs from production
- Much NFF due to different fault spectrum than production test
- Trial-and-error replacement of complex components
- Repair test must be better supported
Goals - Technology View

• Qualified understanding of failure mechanisms at all levels and during the life span
• Capability to predict failures in new technologies
• Control over design verification; coverage, uncertainties, margins
• Achieving a more failure focussed test
Goals - Methodology View

- A life cycle perspective to testing is required
- Proactive engagement in early design phases to plan test and supervision implementation
- Established methods and building blocks to support test - DFT reuse
- Tools and methods to support both HW and SW BIT implementations, including trade-off support
- Composite coverage calculation must be solved
Goals - DFT View

• Architectures and concepts for self test implementation at all levels
• A hierarchical DFT concept
• SoC HW and embedded SW as a DFT platform for board and node test
• Qualified test/DFT support needed
RBS DFT Example
A Systems View of Test and DFT

Test and DFT for SoC
Technology

- CMOS 0.15 um and smaller, 3 M gates + memory
- Al -> Cu metallization
- On-chip SRAM, DRAM introduced
- uP cores, DSP cores and other IP on-chip
- Several PLLs and clock domains
- Gated clocks
- Proprietary DFT and debug features
TARAC Floorplan

Figures of Merit:

- Logic: 1731 kGates
- SRAM: 3448 kBit
- FlipFlops: 51 k
- Transistors: 27.5 M

Performance: >3000 MIPS

Max useful power: 4.1 W
(Theoretical max 6.4 W)

304 HBGA Package
230 Active I/O pins
75 Power pins

DSP Core Size
2.69 x 2.75 = 7.56 mm²
162 kGates
6.5 kWord SRAM

Chip Core Area
11.6 x 12.2 = 141.5 mm²
~ 18% routing

Logic Density in Global Blocks = 35 kGates/mm²

Total Chip Area Including Padring
12.02 x 12.52 = 151.7 mm²

VSC10p38 Pad
81.6 μm wide
210 μm high

Contents of Area
DSP1
DSP2
DSP3
DSP4
DSP5
DSP6
DSP7
DSP8

31 kGates
320 μm²
200 nF

51 kGates
462 μm²
50 nF

17 kGates
42 μm²
10 nF

20 kGates
66 μm²
10 nF

8.5 kGates
250 μm²
10 nF

3 kGates
220 μm²
10 nF
Test and DFT

- Scan mainstream for digital
- Memory BIST of different flavors
- Logic BIST ramping up, scan based
- Hard uP cores tested with proprietary DFT and vectors
- Small set of functional vectors
- A handful of IDDQ vectors
- PLLs tested with vendor methods
- Analog tested functionally
IDDQ Test

![Diagram of IDDQ Test](image)
Test Problems

- Scan vectors hardly fits in tester memory
- Scan vectors does not hit all CMOS defects
- IDDQ will not work for very large ICs
- Signal integrity becoming a problem
- Hard core testing awkward
- Test execution time increases rapidly, +10 s
Implementation Forecast

• Feature sizes decreasing, causing more leakage, lower yield, more metal migration, more soft faults
• Reuse of building blocks major design practice
• More heterogeneous chips, including analog, FPGA and flash memories
• Major chip area will be memories
• Long inter-block wires
• Reuse of building blocks major design practice
• IP’s will appear in hierarchies
BIST Requirements

• More efficient logic BIST
• New techniques for on-chip DRAM and SRAM test and repair, dual mode BIST
• BIST for Flash, FPGA etc.
• BIST for analog: PLL, A/D, D/A, etc.
• Interconnection BIST
• BIST both HW and SW implemented, support
STUMPS - Serial BIST

CUT = Circuit Under Test
BSR = Boundary Scan Register
PO, PI = Primary Output/Input
ISR = Internal Scan Register
Test Register Selection

Parallel BIST
DFT Requirements

• P1500 access and isolation
• User defined test access mechanism (TAM) strategy
• Test scheduling, driven by test time, power dissipation, DFT resource and test bus sharing, etc.
• Test controller and external access
• Management of test instructions at several levels of abstraction
• A common test and DFT architecture (HW+SW) to facilitate reuse and distributed design
Blocks with Different Test Properties

- HARD W. VECTORS
- HARD W/O VECT.
- MEMORY WITH ALGORITHM
- SOFT W/O VECT.
- PROCESSOR WITH MULT. BIST FEATURES
- UDL WITH BIST
- SOFT W/O VECT.
Boundary Scan

- HARD W. VECTORS
- MEMORY WITH ALGORITHM
- PROCESSOR WITH MULT. BIST FEATURES
- UDL WITH BIST
- SOFT W/O VECT.
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- SOFT W/O VECT.
- SOFT W/O VECT.
Test Isolation/Access Collars around Blocks
IEEE P1500
Test Bus Linked to Boundary Scan TAP
DFT for Block Test
DFT for Board/System Level Test
Embedded Test Controller
SoC DFT Architecture

Embedded Test Controller
- IP-BIST1
- IP-BIST2
- IP-BIST3
- Chip-ID
- MemBIST
- Test I/F Controller
- FuncTestuP
- TestIP-1
- TestIP-2
- TestIP-3
- TestIP-4
- FChecksum

Syst. I/F
- uP

DRAM
- IntIP
- ExtIP

FLASH
- IntIP
- P-BIST

RAM
- IntIP
- RAM
- RAM
- RAM
- RAM

I/F Controller

Diagnostic access

Board busses
LBIST Design Flow Today - Block Level

- Run Synopsys’ Design Compiler with scan insertion, but without scan routing
- Run rules checking, correct violations
- Check fault coverage
- Run test-point insertion and scan routing
- Generate signature and test bench
- Run unit delay simulation
- Run static timing simulation analysis on the BIST ready block
LBIST Design Flow Today - Chip Level

- Do chip level functional integration
- Connect scan chains to the scan router block
- Run rules checking, correct violations
- Generate clock pre-scaler, PRPG, MISR, BIST control, boundary scan cells, TAP, instruction decoder, etc.
- Add manually private instruction logic and DFT
- Verify
Design Flow Requirements

• Well integrated DFT tools:
  • Rules checking linked to behaviour/RT descriptions
  • Test points inserted at synthesis
• DFT tools at block level manageable by designers
• Both BISTed and BIST-ready support at block level
• Flexible and comprehensive
  chip level integration support
• Flexible test controller design support
• Minimal DFT rework at ECO, w.r.t. both block and
  chip levels