FDA125 Advanced Parallel Programming February 2007

Exercises for Topic V (Distributed Shared Memory)

Exercise V.1

Consider a simple uniprocessor system with no caches. How does register allocation (applied by the compiler) affect memory consistency? Which language feature of C allows you to enforce sequential consistency for a variable?

Exercise V.2

Assumes that shared variables x and y happen to be placed in the same memory page of a DSM system. The parallel program contains a (asynchronous) loop with n iterations where processor P_1 reads variable x in each iteration and processor P_2 writes y in each iteration.

(a) How many messages are to be sent if sequential consistency is to be enforced?

(b) Show how thrashing can be avoided by using a relaxed memory consistency model.

(c) Which optimizing compiler transformation could be applied to this loop if sequential consistency for x and y is abandoned?

Exercise V.3

Consider a superscalar RISC processor running at 200 MHz. Assume that the average CPI (clock cycles per instruction) is 1. Assume that 15% of all instructions are stores, and that each store writes 8 bytes of data. How many processors will a 1-GB/s bus be able to support without becoming saturated?