TDTS10:
Computer Architecture

Lesson

2024

LINKÖPING UNIVERSITY

Outline

- Lab organization and goals
- SimpleScalar architecture and tools
- Exercises

Organization

- Assistants
  - Group A, B: Yungang Pan
  - Group C, D: Ayla Babazade

- Web page
  - http://www.ida.liu.se/~TDTS10
  - Check the lab page!

Organization

- Sign up in Webreg, deadline: Nov. 14.
- Deadline for handing in lab reports:

Lab 1	Nov. 29
Lab 2	Dec. 13
Lab 3	Dec. 27

- Rules: Read them!

Lab Schedule

Lab schedule for groups
A (by Yungang) and C (by Ayla)

Date	Time	Location*	Type
Nov. 12	13:15–15:00	A33(A), A34(C)	Lesson
Nov. 14	08:15–10:00	SU00(A), SU12(C)	Lab
Nov. 22	15:15–17:00	SU24(A), Olympus(C)	Lab
Nov. 26	13:15–15:00	SU01(A), SU00(C)	Lab
Dec. 2	10:15–12:00	Olympus(A), SU04(C)	Lab
Dec. 13	15:15–17:00	SU01(A), SU00(C)	Lab
Dec. 18	08:15–10:00	Olympus(A), SU24(C)	Lab

***SU04(A) means that the students of group A should go to room SU04.**

Lab schedule for groups
B (by Yungang) and D (by Ayla)

Date	Time	Location*	Type
Nov. 12	13:15–15:00	A33(B), A34(D)	Lesson
Nov. 15	15:15–17:00	Asgard(B), Egypt(D)	Lab
Nov. 19	13:15–15:00	SU01(B), SU00(D)	Lab
Nov. 28	08:15–10:00	SU01(B), SU00(D)	Lab
Dec. 5	10:15–12:00	Olympus(B), Roxen(D)	Lab
Dec. 9	10:15–12:00	SU01(B), SU00(D)	Lab
Dec. 16	10:15–12:00	SU04(B), Olympus(D)	Lab

***SU04(B) means that the students of group B should go to room SU04.**

Please only attend your own lab sessions (6 sessions)

Please check the lab location from these tables (available on webpage).

Examination

For each lab:

1. Demonstrate
   - Must be done during lab sessions
   - Both members must be present during demo
2. Report, Submitted via EMAIL

Labs

- Three labs:
  1. Cache Memories (2 lab sessions)
  2. Instruction Pipelining (2 lab sessions)
  3. Superscalar Processors (2 lab sessions)

Goals

- Obtain knowledge about computer organization and architecture
- Insights in various trade-offs involved in the design of a processor
- Become familiar with a set of tools necessary for evaluation of computer architectures

Environment

- Linux
- Simulations are started from a command line (i.e., terminal)
  - To open a new terminal you can press ctrl+alt+t
- Get yourself familiarized with the terminal
  - Ask Google first
  - Ask your assistant
- Make sure you learn the basic commands (i.e., *cd, ls, cp*, …)

Tool Setup

- Don’t forget the instructions in lab0
- Instructions should be clear and easy to follow, but if you face difficulties
  - Don’t get frustrated :)
  - Read again carefully (without skipping over the lines)
  - Consult your assistant

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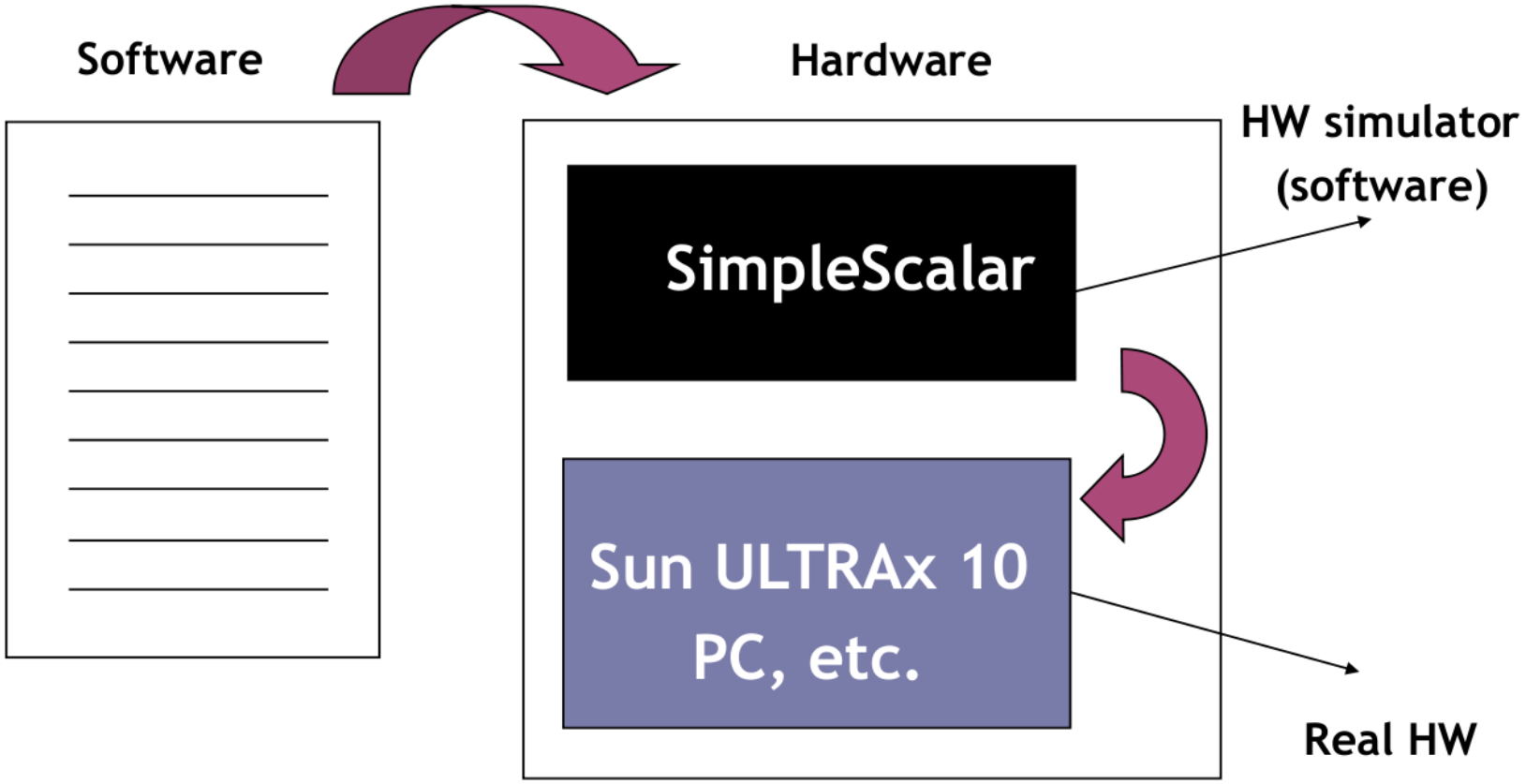
Architecture Simulation



SimpleScalar: Literature

- "*The SimpleScalar Tool Set, Version 2.0*", by Doug Burger and Todd M. Austin
  - Very important preparation for the labs
  - This is your main reference for the tool!
- "User's and Hacker's guide", slides by Austin

SimpleScalar Architecture

- Virtual architecture derived from MIPS
  - Control (j, jr,..., beq, bne,...)
  - Load/Store (lb, lbu, ...)
  - Integer Arithmetic (add, addu, ...)
  - Floating Point Arithmetic (add.s, add.d, ...)
  - Miscellaneous (nop, syscall, break)

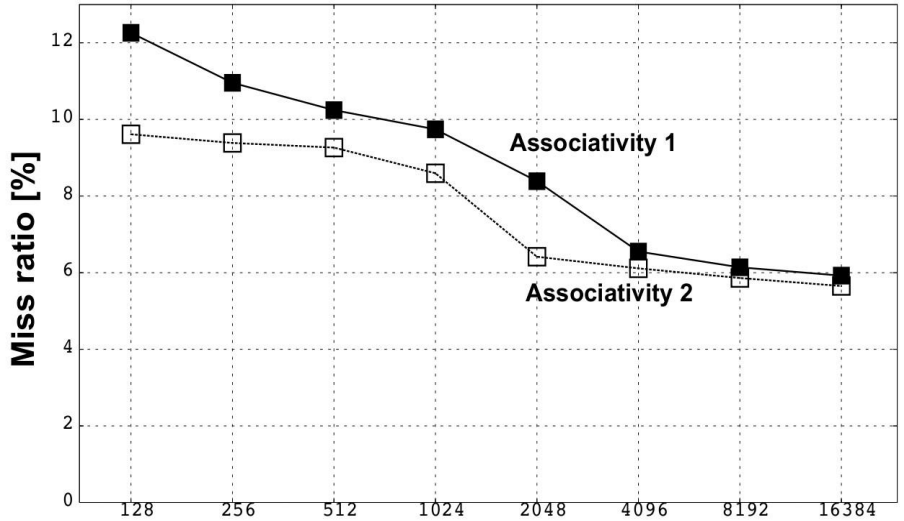
SimpleScalar Architecture (cont'd)

- Several simulators
  - Sim-fast: Fast, only functional simulation (no timing)
  - Sim-safe: Sim-fast + memory checks
  - Sim-cache: Sim-safe + cache simulation and various timing properties (simulation time, measured time, ...)
  - Sim-cheetah: Simulation of multiple cache configurations
  - Sim-outorder: Superscalar simulator

Won't use these two!

An Example

- Lab1, assignment 3
  - Dump the default configuration of sim-cheetah
  - Modify the configuration and simulate
  - Plot the results (e.g. OpenOffice, Gnuplot, Matlab, Excel)



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- Lab organization and goals
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- Let’s solve some exercises on the first lab!
  - Lesson exercises