Aim

The purpose of the course is that students shall acquire knowledge on the importance of design of testable digital systems and develop the ability to formulate and solve problems related to testing. After completing the course, students shall be able to:

- describe for fundamental test and fault concepts
- methodically solve test related problems in a development environment
- formulate and implement/apply test algorithms
- define and implement a minor design-for-test assignment

Recommended Textbook

The recommended textbook is:


Personnel

Erik Larsson - Course leader (examinator)
- Email: erik.larsson@liu.se
Dimitar Nikolov - Course assistant
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Madeleine Häger Dahlqvist - Course secretary
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Alternative Literature


Survey/tutorial papers

- Design for testability - A survey, Williams, T.W. and Parker, K.P.
- Resource-constrained system-on-a-chip test: a survey, Xu, Q. and Nicolici, N.

Examination

TEN1: Written exam (U,3,4,5), 3 ECTS
- Written examination (max 40 (including 10 points from labs) points)
  - 5=A=34p
  - 4=B=28p
  - 3=C=22p
  - UK=Fx=less than 22p
LAB1: Laboratory work - 3 ECTS
- Can get up to 10 points to include in the written pre-exam "Dugga" (note - each dugga is given at one time; no possibility repeat)

Laborations

Registration
- The labs should be solved individually. Registration in WebReg.
- Questions regarding the registration are answered by Dimitar
- Last day for the registration is defined by Dimitar

General instructions
- The labs should be handed in using the covers located by the printers
- Last day of handing in the labs will be told by Dimitar

Instructions and guidelines
- Lab 1 - Test pattern generation
- Lab 2 - Design for test
- Lab 3, 4 - Boundary Scan
Course Outline
- Introduction; Manufacturing, Wafer sort, Final test, Board and System Test, Defects, and Faults
- Test generation; combinational and sequential test generation
- Design-for-Test techniques; test point insertion, scan, enhanced scan
- Built-In Self-Test; Logic BIST and memory BIST
- System Chip Test; test architectures, test planning, test scheduling, and test data compression, power constraints, test data compression.
- System Test and boundary Scan
- Two invited speakers from SAAB
- Study visit to Flextronics

Late Course Registration
- Please find the correct form from: http://www.lith.liu.se/blanketter/
- Fill the form and give it to Patrick Lambrix (director of studies) in office: B 2B:474, Building B, Ground Floor

Outline
- Electronics
- Manufacturing
- Test, diagnosis, and verification
- Cost, defects, fault models, and quality of test
Products with electronic systems

Production of electronic products

Making electronic products

Transistor Count

Types of products:
- First of a kind: product that breaks new ground
- Me too with a twist: improve existing product (example, fast bus)
- Derivate: add a little more functionality
- Next-generation product: replace mature product
Integrated Circuits (ICs)

- Small Scale Integration (SSI), early 1960s, example, Philips TAA320 had two transistors
- Medium Scale Integration (MSI), late 1960s, example, Intel 4004 had 2300 transistors
- Large Scale Integration (LSI), mid-1970s, example, Intel 8008 had 4500 transistors
- Very-Large Scale Integration (VLSI), 1980s, example, Intel 80286, 134000 transistors
- Ultra-Large Scale Integration (ULSI), now, more than 1 million transistors
  - Wafer-scale integration (WSI)
  - System-on-a-chip
  - Three dimensional integrated circuits (3D-ICs)

**IC**

- Viper 2.0 RevB
- Analog/Digital TV Processor
- 10mm x 10 mm (100 mm²)
- ~10 M gates
- ~50 M transistors
- ~100 clock domains

Printed Circuit Board (PCB)

Multi-board system
Types of systems

- Analog systems
- Digital systems
- Mixed signal systems

Digital systems

- AND-gate

Manufacturing
- Viper 2.0 RevB
- Analog/Digital TV Processor
- 10mm x 10 mm (100 mm²)
- ~10 M gates
- ~50 M transistors
- ~100 clock domains

IC manufacturing

Feature size

Lithography has three parts: (1) Light source, (2) Wafer exposure (3) Resist
Bonding Techniques

Outline

- Electronics
- Manufacturing
- Defects, test, diagnosis, and verification
- Cost, defects, fault models, and quality of test

IC Defects

(a) Through-Hole Mounting

(b) Surface Mount
Defects and Faults

- Example of a defect

- A defect manifests itself as a fault
  - Fault: permanent or temporary (in respect to time)
    - Permanent (hard)
    - Temporary (soft)

PCB Defects

<table>
<thead>
<tr>
<th>Defect classes</th>
<th>Occurrence frequency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shorts</td>
<td>51</td>
</tr>
<tr>
<td>Opens</td>
<td>1</td>
</tr>
<tr>
<td>Missing components</td>
<td>6</td>
</tr>
<tr>
<td>Wrong components</td>
<td>13</td>
</tr>
<tr>
<td>Reversed components</td>
<td>6</td>
</tr>
<tr>
<td>Bent leads</td>
<td>8</td>
</tr>
<tr>
<td>Analog specifications</td>
<td>5</td>
</tr>
<tr>
<td>Digital logic</td>
<td>5</td>
</tr>
<tr>
<td>Performance (timing)</td>
<td>5</td>
</tr>
</tbody>
</table>


Test

Device under test (DUT)

Stimulus: test vectors

Stimulus → Response

Test pattern: test vector + expected test response (ordered n-tuple of binary values)

Produced test response is compared against expected test response

Verification, test and diagnosis

- **Verification** is to verify the correctness of the design. It is performed through simulation, hardware emulation, or formal methods. It is performed once prior to manufacturing. Responsible for quality of design.

- **Test** verifies the correctness of manufactured hardware. Test is a two-part process:
  - Test generation: software process executed once during design, and
  - Test application: electrical tests applied to hardware. Test application performed on every manufactured device. Responsible for quality of devices.

- **Diagnosis**: Identification of a specific fault that is present on DUT.
Diagnosis and volume production

Outline

- Electronics
- Manufacturing
- Defects, test, diagnosis, and verification
- Cost, defects, fault models, and quality of test

Making fault free electronic products

Rule of ten: Finding a defect in one later step increases cost with a factor 10 compared to addressing the defect in current step.

Types of Test

- Production
  - Wafer sort (or probe)
  - Final test (package)
- Acceptance
- Sample
- Go/No-go
- Characterization (performance)
- Stress screening (burn-in)
- Diagnostic (repair)
- On-line

Test Preparation | Production Test | In-Field Test
ok? | ok? | ok?
Types of Test

- Wafer sort - tests the logic of each die on the wafer
- Final test - tests the logic of each packaged IC
- Board test - tests interconnections (soldering errors)

Important aspects

- Specify the test vector
- Determine correct response (expected response)
- Evaluate quality of test
- Fault coverage = No of faults detected / No. faults modeled
- Defect level (DL) = Number of faulty units shipped / Total number of units shipped.
- Yield = Number of good parts / Total number of tested parts
- Williams and Brown (1981): DL=1-Y^{(1-T)}
  where Y is yield and T is ratio of covered parts by test.
- For example:
  - If possible to test all defects: T=1 -> DL=1-Y^{(1-1)}=0
  - If no defective units manufactured: Y=1 -> DL=1-1^{(1-T)}=0 (T can be 0)

Manufacturing Test

- Determines whether manufactured chip meets specs
- Must cover high % of modeled faults
- Must minimize test time (to control cost)
- No fault diagnosis
- Tests every device on chip
- Test at speed of application or speed guaranteed by supplier

Testing

- Automatic Test Equipment (ATE)
- Test stimuli (TS)
  - 0010100
  - 0110000
- Expected responses (ER)
  - 1011001
  - 1101010
- Produced responses (PR)
  - 0111011
  - 0100101
- Pass/fail
- Device under test
Tests

- Good IC that pass test -> OK
- Bad IC that fail test -> OK

- Bad ICs that pass test -> test escape
- Good ICs that fail test -> yield loss

<table>
<thead>
<tr>
<th>IC</th>
<th>Outcome of test</th>
</tr>
</thead>
<tbody>
<tr>
<td>Good</td>
<td>Pass</td>
</tr>
<tr>
<td>Bad</td>
<td>Test esc.</td>
</tr>
<tr>
<td></td>
<td>Fail</td>
</tr>
<tr>
<td></td>
<td>OK</td>
</tr>
<tr>
<td></td>
<td>Yield loss</td>
</tr>
</tbody>
</table>

Automatic Test Equipment Components

- Consists of:
  - Powerful computer
  - Powerful 32-bit Digital Signal Processor (DSP) for analog testing
  - Test Program (written in high-level language) running on the computer
  - Probe Head (actually touches the bare or packaged chip to perform fault detection experiments)
  - Probe Card or Membrane Probe (contains electronics to measure signals on chip pin or pad)

Automatic Test Equipment Companies

- Teradyne was founded in 1960 by two classmates from Massachusetts Institute of Technology (MIT). [http://www.teradyne.com/](http://www.teradyne.com/)
- LTX was founded in 1976 and the headquarter is in Norwood, MA (Greater Boston), [http://www.ltx.com/](http://www.ltx.com/)
- Agilent Technologies (formed in 1999 from a division of Hewlett-Packard), [www.agilent.com](http://www.agilent.com)
- Verigy was in 2006 formed from a division of Agilent Technologies, now part os Advantest, [https://www.verigy.com/](https://www.verigy.com/)
Automatic Test Equipments (ATEs)

- Sapphire from Credence
- V93000 from Verigy
- T6577 from Advantest
- Tiger from Teradyne

Fault models

- Stuck-at Fault, Bridging Fault, Shorts (Resistive shorts), Opens, Delay Faults, Transient Fault
- So far stuck-at fault model is the most used one:
  - Motivations:
    - Simple
    - Covers quite well possible defects
  - Above 65 nm: SA0 and SA1
  - At 65 nm -> TSMC standard: 6 fault types; DC-SA0/SA1, AC-input slow to rise (ISR), input slow to fall (ISF), output slow to rise (OSR), output slow to fall (OSF)
  - Below 65 nm (i.e. 45 nm and 32 nm): ??

Test generation

Example: Create test for output connected to $V_{dd}$

Fault-free

```
1
```

Faulty

```
1 & 1 \\
1 & V_{dd}
```
Test generation

Example: Create test for output connected to $V_{dd}$

<table>
<thead>
<tr>
<th>Fault-free</th>
<th>Faulty</th>
</tr>
</thead>
</table>
| $\begin{array}{c}
X 0 \\
& & 0 \\
\end{array}$ | $\begin{array}{c}
X 0 \\
& & 1 \\
\end{array}$ |

Find test stimuli such that test responses are different in fault-free and faulty device.

Stuck-at Fault

- A line is fixed to logic value 0 (stuck-at-0) or 1 (stuck-at-1)
- For the stuck-at fault model there are for a circuit with $n$ lines $2^n$ possible fault sites

Quality of a test is given by:

$$\text{fault coverage} = \frac{\text{faults detected}}{\text{total number of faults}}$$

Example: 10 lines (20 faults) detect 12 faults: f.c. = 12/20 (60%)

Single Stuck-at Fault

- Three properties define a single stuck-at fault:
  - Only one line is faulty
  - The faulty line is permanently set to 0 or 1
  - The fault can be at an input or output of a gate
- Example: XOR circuit has 12 fault sites ($\bullet$) and 24 single stuck-at faults
  
  Test vector for faulty circuit value
  
  Good circuit value
  
  Faulty circuit value

Example: XOR circuit has 12 fault sites ($\bullet$) and 24 single stuck-at faults