# VILAB Project: WUT Progress Information

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# Agenda

- ◆ What we have done
- **◆IMiOVIP** Tutorial
- **◆ Future works**

### **IMiOCAD Development**

(Subtask 2.5)

- New versions of all IMiOCAD tools (versions for Wintel and Unix platforms under development)
- ◆ User's Manuals available for download
- ◆ New technology files for IMiOCAD tools for Alcatel C07M and AMS CYE, BYE and CSD processes

# Fault probability estimation tool

(Subtask 2.6)

- ◆ A tool for estimation of probability of spot defectrelated faults in digital standard cells is under development
- ◆ Work is carried out in co-operation with Tallinn TU and Lviv Polytechnic (not VILAB partner)

# IMiOVIP - virtual prototyping tool accesible via Internet

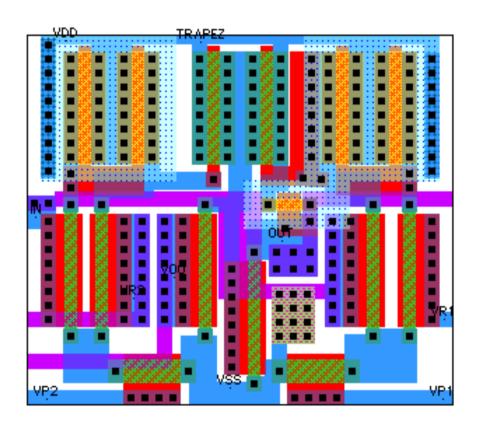
(Subtask 2.6)

◆ First simulation tool of **IMiOVIP** - an interactive process and device simulator - is already available for VILAB partners on the Internet (http://imiovip.imio.pw.edu.pl)

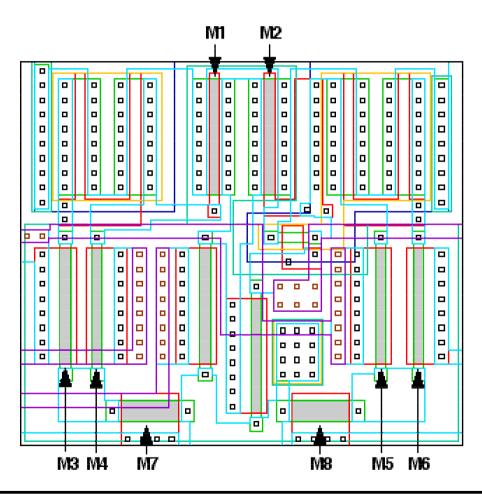
#### **IMiOVIP** tutorial

- ◆ Run circuit extractor on layout of validated cell
- ◆ Select the devices to be simulated
- ◆ Enter the device dimentions and location
- ◆ Run statistical process/device simulation
- ◆ Obtain results in form of plots

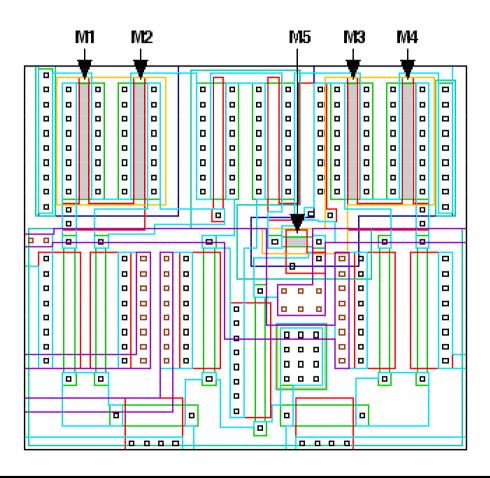
# Tutorial - layout of validated cell



#### **Tutorial - NMOS transistors extracted**



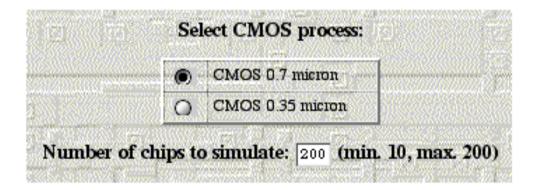
#### **Tutorial - PMOS transistors extracted**



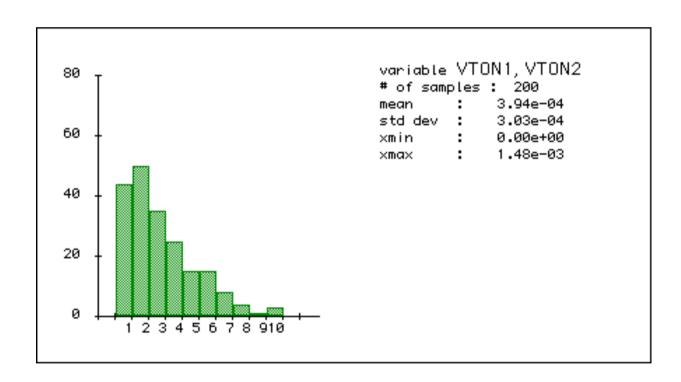
# Tutorial - transistor size/location setup

n-MOS (n channel) transistors:				
Transistor data :	Width (um):	Length (um) :	X (um)	Y (um)
Transistor 1: 🗹	20.0	2.0	32.25	43.0
Transistor 2: 🗹	20.0	2.0	41.75	43.0
Transistor 3: 🗹	2.0	20.0	6.75	14.0
Transistor 4: 🗹	2.0	20.0	12.25	14.0
Transistor 5: 🗹	2.0	20.0	60.75	14.0
Transistor 6: 🗹	2.0	20.0	67.25	14.0
Transistor 7: 🗹	4.0	10.0 agus c	17.25	4.0
Transistor 8: 🗹	4.0	10.0	46.5	4.0
Transistor 9: 🗌	1.0	1.2	0	0

## **Tutorial - process selection**



#### **Tutorial - simulation results**



#### **Future works**

- ◆ Internet-based tutorials for IMiOCAD tools
- IMiOCAD demo versions for download
- ◆ IMiOVIP development: coupling layout-to-circuit extractor with process simulator
- ◆ IMiOVIP for IET process
- Improvement of faults probability estimation method