Call for Participation in a SYDIC-Training Course on

**Functional Verification for VLSI**

**Course Contents**

**What is Verification?**
- What constitutes verification, what’s its purpose, and what is the interdependence of and independence between design and verification? An overview of the typical phases of planning and execution. An overview of tools, languages and techniques

**Verification Methodology**
- What is the organisational context of verification? Successful methodology depends upon good practise. Various tool/language decisions required in practical verification. Characterisation of the different types of verification.

**Project Verification Strategy**
- Covering project-specific methodology and strategy that needs to be defined depending upon the nature of project. For example, how the target technology (FPGA/ASIC) or target application area might determine the verification approaches used.

**Project Verification Plan**
- Feature extraction, Coverage driven verification, Classifying and sorting, Effort and resource estimation — engineers, licences, compute power, allocation, Milestones

**Project Verification Execution**
- Issue tracking and bug profiling, completion criteria, Post-mortem

**Testbench Writing Overview**
- Determining the correct level of interface abstraction, Identifying components within testbench structure, Testplan-driven functional requirements

**Data Generation and Reassembly**
- Design and generation of data structures for DUV input, Reassembly of data structures from DUV output, Data structure APIs

**Objective**
Provide participants with a good basic knowledge of VLSI functional verification methodologies. The emphasis is on the practical aspects of the planning and execution of functional verification of complex digital ASIC/FPGA designs.

**Target Audience**
Design Engineers, and Software Engineers wanting to expand their knowledge of basic verification. Would also suit engineers with EDA knowledge.

**Duration**
4 days

**Dates**
9-12 June 2003

**Venue**
Institute for System Level Integration, ISLI
Automated Self Checking

- Definition of automated self checking, Selection/implementation of reference models, Protocol monitors, Scoreboards, Register mirrors

Bus Functional Models and Verification Components

- Bus functional models (drivers), Mail boxes, queues, stacks, Logging and error handling, Timeouts, API issues

Overview of Formal Verification

- Proof vs simulation, Formal specification and degrees of abstraction, Overview of formal verification activities, Overview of formal verification technologies, Advantages and limitations of formal verification, Bug finding vs correctness

Equivalence Checking and Simple Property Checking

- Formal equivalence checking, including usage of Binary decision diagrams, Basics of property specification (assertion) languages, behaviour over a specified number of clock cycles

Advanced Property Checking

- Linear-time and branching-time temporal logics, Linear-time properties about behaviour over an unspecified number of clock cycles, Properties at higher levels of abstraction, Deductive theorem proving

Complexity Management

- Sources of complexity within the VLSI verification tasks and describes some common tools and methods used to manage this growing problem

Verification Automation

- Machinery and reasons behind the automation in large-scale design verification, techniques borrowed from the software engineering disciplines

Case Study — Verification of an ARM-based SoC

- Case study in the verification using an ARM-based SoC design, paying particular attention to the AMBA bus architecture and protocol compliance checking. The design is verified using a high-level verification language (Specman Elite) and uses the Rapier SoC design from the ISLI’s database.

Costs

SYDIC Training partners may be eligible for free places, please consult course organiser.

The course is given in the framework of the EU project IST-2001-35100 SYDIC-Training. Additional information can be found at www.ecsi.org

Organizer

Mrs. Avril Manners

Registration and contact

suzanne.o'hare@sli-institute.ac.uk

Online

www.sli-institute.ac.uk

Address details

Institute for System Level Integration
The Alba Centre
The Alba Campus
Livingston, EH54 7EG
Scotland.

Phone: +44 (0) 1506 469300
Fax: +44 (0) 1506 469301
E-mail: suzanne.o'hare@sli-institute.ac.uk

Directions for travel to ISLI may be found at http://www.sli-institute.ac.uk/img/nav_contacts_ovr.jpg