STRINGENT Projects March 2006

Short descriptions of running projects, related to the different research groups, Computer engineering (Da), Electronic devices (Ek), Embedded systems (Em) and Electronic systems (Es). For each project group there is one responsible researcher (group leader). His name is given in the list below, and his tasks are defined after the list.

Structured list of projects.

System design

Networks-on-chip (Christer Svensson)

Da1 SOCBUS

Em1 Optimization of real-time applications implemented on power constrained network-on-chip architectures

Em8 Heterogeneous networked embedded systems

Heterogeneous multiprocessor systems (Dake Liu)

Da2 Programmable IP routing core for future core networks

Da3 High end flexible DSP processor for future media trans-coding

Da5 Low power base-band processor for SDR (Soft Defined Radio)

Em6 Design of heterogeneous multiprocessor systems for real-time applications

Signal processing algorithms (Lars Wanhammar)

Es4 Integrated active filters

Es5 Design and Implementation of Energy Efficient Digital Filters

Es6 Low-Complexity Digital Filters and Filter Banks

Es7 Estimation, synchronization and equalization algorithms

Es8 Low Power Algorithm Design and Implementation

Technology utilization

High speed interfaces (Jerzy Dabrowski)

Ek2 High speed off-chip communication

Ek5 Wide-band or tunable low noise amplifiers

Ek11 RF frontened design for software defined radio

AD and DA converters (Mark Vesterbacka)

Es2 Reduction in substrate noise in mixed-signal circuits

Es3 High performance ADCs implemented in SOI technology

High performance, low power circuit techniques (Atila Alvandpour)

Ek7 Low Power Multi-GHz Clocking

Ek8 Embedded Memories

Ek9 System On-Chip Synchronization and Communication Techniques

Ek10 Low Power, High Performance Processor Building Blocks

Efficient design

Verification (Petru Eles)

Em4 Formal verification of embedded systems in a reuse methodology

Testing (Zebo Peng)

Ek6 Testability-oriented design techniques for mixed-signal/RF integrated circuits

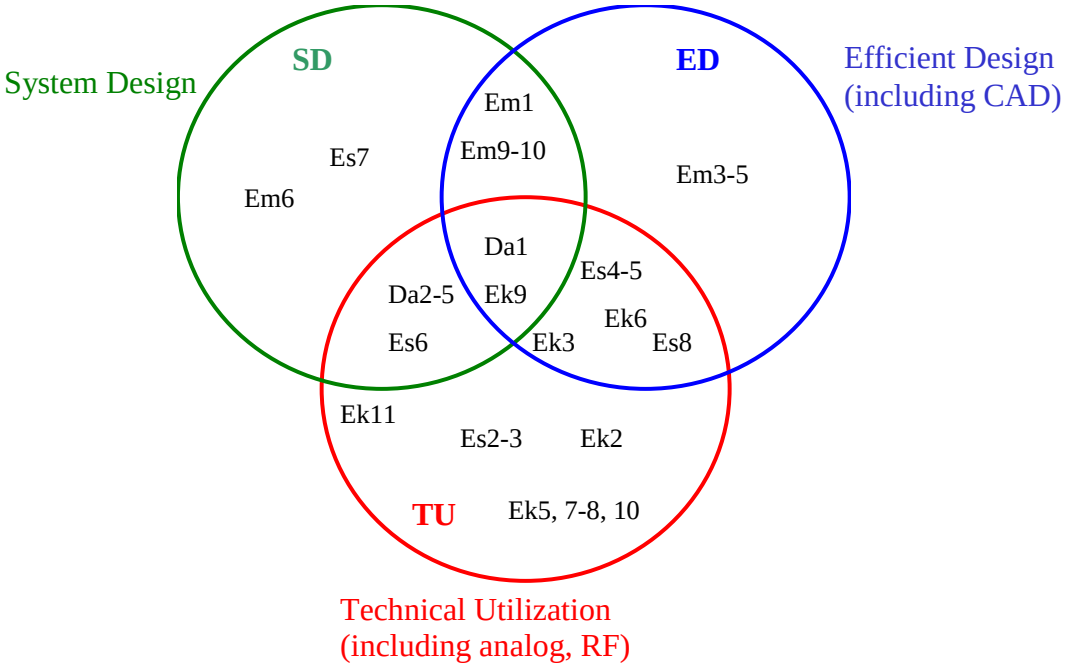
Em3 Hybrid BIST methodology for complex electronic systems

Em5 Testing system-on-chips using functional bus

Em9 SoC wrapper design, TAM configuration and test scheduling

Em10 Analysis and design of fault-tolerant embedded systems

Positioning of projects into STRINGENT goals:



STRINGENT Projects March 2006

Short project descriptions, related to the different research groups, Computer engineering (Da), Electronic devices (Ek), Embedded systems (Em) and Electronic systems (Es). The projects are organized into project groups.

System design

Networks-on-chip (Christer Svensson)

Da1 SOCBUS

(Qun Ge, PhD student, Dake Liu, supervisor)

Objective: The project was initialized August 1999. Objectives of the project are to develop a platform for SoC integration, to demonstrate the functionality and performance of a novel flexible high bandwidth and low latency on-chip network, and to prove a synthesis based system integration methodology.

Results: The project is going on well. The SOCBUS simulator was developed. Using the simulator, we have got a deep understanding on the deadlock free network and other SOCBUS behaviors. At the same time, we are working on both the SOCBUS functional design and the related physical issues. The simulation result on an 8X8 2D mesh with 64 nodes include: Theoretical limit is 224 “data”/clock cycle; Real system limit is ~40 “data”/clock cycle; we reached 15 “data”/cycle with 10% reject; Finally, the route latency is 20 “system clock cycles”. Results show the performance of our bus keeps the leading position. Seven papers were published during 2000-2002.

Degree of success: The SOCBUS has proven very promising and has been accepted as the SOCBUS project at Acreo. Philips shows high interests in the project. We hope to establish a general SoC integration methodology based on our SOCBUS concept for Swedish communication infrastructure companies.

Em1 Optimization of Real-Time Applications Implemented on Power Constrained Network-on-Chip Architectures

(Alexandru Andrei, PhD student; Petru Eles, Zebo Peng, supervisors)

Objectives: Networks on chip will only be efficiently used if the architecture platform is customized to meet the computation and communication particularities of a certain family of applications. When implementing an application, the problem is how to map the functionality on the existing platform such that constraints regarding cost, performance, and power consumption are satisfied. Therefore, system level design tools for efficient implementation of network-on-chip applications have to be based on accurate delay and power models for the processor cores, memory elements and communication infrastructure. Using such a model to design a good interconnect structure is particularly interesting, in the context in which communication aspects are becoming more and more dominant with the current and future technologies. Accurate power models have to be incorporated in system level routing, scheduling and mapping strategies in order to achieve power efficient implementations that provide the required quality of service. We assume that chips will run at variable, adjustable voltage levels (which is the case with some existing chips already), and that different voltages can be simultaneously used to run parts of the network on chip platform. Further, we will show that communication speed can be dynamically varied, opening the door for optimization. In this context we plan to develop algorithms and tools for mapping and scheduling of communications and computations and for dynamic voltage scaling in the context of performance and power constraints.

Expected Results: We will develop accurate delay and power models for the processor cores and communication infrastructure, as well as algorithms for optimization of real-time applications, implemented on power constrained network-on-chip architectures.

Em8 Heterogeneous Networked Embedded Systems

(Traian Pop, PhD student; Paul Pop, researcher; Zebo Peng, Petru Eles, supervisors)

Objectives: There are several application areas today where architectures consist not only of heterogeneous processing elements, but also of heterogeneous networks. Heterogeneous-network architectures consist of multiple clusters (network of several processing elements sharing one communication infrastructure and protocol) interconnected via gateways. The objective of our research is to guarantee the timing properties of applications described using mixed-formalisms and mapped on such multi-cluster architectures. Timing properties are described either as strict deadlines that have to be met, or as quality-of-service properties.

Results and current work: First, we have developed schedulability analysis algorithms for bus-based heterogeneous time/event-triggered distributed embedded systems. Second, we have developed similar techniques for multi-cluster systems composed of time-triggered (TT) and event-triggered (ET) clusters. The next step will be to develop such approaches for guaranteeing the timing properties of multi-cluster systems with heterogeneous TT/ET processing nodes and heterogeneous communication protocols.

Degree of success: We have received very positive feedback from our industrial partner, Volvo Technology Corporation, and we will continue the cooperation with them in this area. We have also published so far two research papers in this area.

Heterogeneous multiprocessor systems (Dake Liu)

Da2 Programmable IP routing core for future core network

(Anders Ehliar, PhD student, Dake Liu, supervisor)

Objective: The project was initialized August 1999. The goal of the project is to find a way to design programmable network processors for network infrastructure and terminals. To decrease the memory cost and process latency, we need to have line speed processing for high speed network and to eliminate the in-buffer.

Results: Special processor architecture is introduced for data flow dependent control without pipeline penalty. The function design of the demonstrator of the processor is ready December of 2002. The demonstrator will be implemented before March 2003. One Licentiate defense was in December 2001. One Ph.D. thesis will be ready in 2003. One US patent is pending. Sixteen papers were published during Aug 1999 – Dec 2002.

Degree of success: While moving more system jobs into one silicon chip, more opportunities are moving away from Sweden. We try to promote advanced engineering research in this area in Sweden. Ericsson UAB shows great interested in this project. They believe our research is useful for future integrated communication infrastructures.

Da3 High end flexible DSP processor for future media trans-coding

(Per Kalmström, Francisco Rivas, Johan Eilert, Di Wu, PhD students, Dake Liu, supervisor)

Objective: The project was initialized during 2002. The goal of the project is to find algorithms, arithmetic, and processor architecture for audio decoders (layer I to III) to use only 16-bit native length and reach 24-bit or higher audio quality.

Results: We have generated a variable data width behavior model for audio decoding. We have investigated possibilities to reach high audio decoding quality based on optimized mantissa and special exponent coding. A full 16-bit audio decoder behavior modes shows the feasibility to reach high audio quality based on very low memory and very low power.

Degree of success: We demonstrate a way to reach low power on architecture level. Extremely low silicon area gives the opportunities or different down load audio, such as down load audio accelerator for 3G phones, low cost audio terminal behind for ADSL applications.

Da5 Low power base-band processor for SDR (Soft Defined Radio)

(Anders Nilson, PhD students, Dake Liu, supervisors)

Objective: The project was initialized during 2002. The goal of the project is to converge algorithms, arithmetic, and architectures for different radio base band signal processing, including fast fading and slow fading channels; high symbol rate and slow symbol rate channels; as well as different modulations.

Results: We have investigated the requirements on flexibility focusing on base-band. We made a FFT/DCT/DWT converged processor for low power low computing latency applications. We will make a base-band vector processor based on FFT/DCT/DWT converged processor to cover all possible base-band processing before FEC (Forward Error Correction).

Degree of success: The current different advanced base-and DSP base-band solutions are implemented based on custom ASIC. It is necessary to converge these ASIC into a base-band processor. In the last 10

years, GSM has reached 100% programmability. About 10 years from now, all radio base-band should be converged and programmable.

Em6 Design of Heterogeneous Multiprocessor Systems for Real-Time Applications

(Sorin Manolache, PhD student; Petru Eles, Zebo Peng, supervisors).

Objectives: The objective is the development of a methodology for the early design phases of complex heterogeneous multiprocessor systems for real-time applications with a focus on telecommunication applications. The main challenge is the development of fast and accurate performance estimation tools in the context of high uncertainty about design parameters such as processor architecture, task execution times, task mappings, communication architecture and communication protocols. We propose a probabilistic approach to the analysis of such systems.

Results: Two analytic approaches have been proposed for the performance estimation (schedulability analysis) of real-time systems in the context of stochastic task execution times. They have been published in two conference papers. The results are also available in the licentiate thesis of Sorin Manolache. Both approaches provide the expected deadline miss ratio on a per task or task graph basis given a set of annotated task graphs, a mapping, a scheduling policy, and a set of task execution time probability density functions. The first approach is an exact one, and is efficiently applicable to monoprocessor systems. The second approach is applicable to both mono and multiprocessor systems and provides an approximate solution where the designer may trade, in a controlled way, analysis speed for analysis accuracy.

Signal processing algorithms (Lars Wanhammar)

Es4 Integrated active filters

(Emil Hjalmarson and Robert Hägglund, PhD students, Lars Wanhammar, supervisor)

Objective: Traditionally, analog circuit design is a time consuming and difficult task due to the complex relations between performance measures and design parameters. Analog design is therefore sometimes looked upon as a black art in electronics where lose and vaguely defined design methodologies are used.
In this project the aim is to change this situation by introducing a well-defined path for analog design. The work involves the development of analog design automation tools to reduce design times and increase performance and robustness. In this way we aim at bridging the gap between analog and digital design efficiency that exist today. Our focus is on the design and implementation of high-performance integrated analog circuits, filters, and filter banks for use in analog/digital interfaces, anti-aliasing and reconstruction filters in A/D and D/A converters, etc. However, the concepts developed within this project can be applied to virtually all analog and RF circuit designs.

Results: The focus of the work have been on the development of analog design automation tools. Particularly the part of determining device sizes to meet a performance specification have been treated. However, the work also includes methods for exploring the analog design space, layout generation and compensation for layout dependent parasitics. The device-sizing tool uses an equation-based approach to solve the sizing problem. However, the tool has been improved in several areas compared to traditional equation-based approaches. For example, a short setup time is achieved trough the use of a symbolic analyzer approach where the symbolic performance equations are derived automatically from a user specified circuit topology. The topology can be drawn in tradition design tool such as Cadence and performance measures are defined using a traditional test bench setup. High accuracy performance predictions, comparable to SPICE simulations, are obtained through the use of high-accuracy transistor models. The optimization algorithms used are capable of finding good circuit solutions without a good initial starting point. Further, to ensure robust solutions with respect to process variations yield enhancement techniques are applied.

The tool has been successfully used to design large operational amplifiers (100 transistors) within reasonable time. A complete RC filter with about 200 devices suitable for ADSL applications have also been designed. Here the results show that significant improvements in terms of design time and performance can be obtained by considering the whole filter at once instead of using a divide and conquer technique. The device-sizing tool has also been used to perform extensive design space exploration where several circuit topologies are compared and the effect of changing the circuit specification can easily be investigated. Visualization of, e.g., the power consumption vs. area for different sets of power supply voltages are possible. Such information can be used to trade area for power consumption in order to obtain circuits that are better suited for the application of interest.

A simple template-based layout tool has been implemented in order to evaluate the concept of parasitic feedback. In parasitic feedback from the layout are extracted and feed back annotated into the device-sizing tool. Using an iterative procedure the sizing tool is able to redesign the circuit to meet the specification when these parasitics are present.

Es5 Design and Implementation of Energy Efficient Digital Filters

(Henrik Ohlsson, Kenny Johansson PhD student, Oscar Gustafsson, co-supervisor, Lars Wanhammar, supervisor)

Objective: In this project we develop efficient design methods and adapt commercial tools for design of low-power DSP systems and subsystems with given throughput requirements. More specifically, the DSP application considered is various forms of multirate digital filters with high throughput and low power consumption. The target applications are high-volume, low cost integrated DSP systems/components. Typical examples can be found in communication systems both on radio and copper wires. These systems

will typically have high, or very high, throughput and at the same time operate on a stringent energy budget, which means that power consumption and energy efficiency are major design issues at all levels of the design flow. Further, the development time must be very short since these systems are consumer products. Hence, the development technique is also of major importance. Multirate digital filters are important components in most DSP systems. Such filters are, for example, often required in A/D and D/A converters. Conventional high-speed decimation and interpolation digital filters consume about the same power as an A/D converter. Hence, implementations that are more efficient are required in order to allow a larger part of the power budget to the analog circuitry, which can not take advantages of reduced geometries. We are one of the leading groups in the world in design and implementation of digital filters and during the last few years we have proposed a large number of novel filter structures that address these applications. However, the new structures must be evaluated by comparison at the hardware level of their performance in terms of design effort, maximal speed, and power consumption. Further an efficient design flow must be developed since there are many possible variations. To improve the design efficiency and reduce the filter implementation times, an efficient design flow for digital filters is under development. This design flow covers the entire design process, from the filter specification down to the filter implementation.

Results: Several different algorithms for the multiple-constant multiplication (MCM) problem have been presented. Novel power estimation methods for adders and multipliers have been developed, taking the correlation between adjacent samples into account. Cooperation with the Division of Information Theory has been established. Several joint papers have been published or are in the pipeline. A very high-speed decimation filter has been implemented and successfully processed utilizing a novel low power architecture. The work on the design process has continued, mainly with automated synthesis of MCM blocks and digit-serial FIR filters. An efficient method for computing sine and cosine has been developed with an optimization framework and improved architectures. This method is currently generalized and evaluated for approximation of other elementary functions. Furthermore, Henrik Ohlsson presented his PhD Thesis in May. A detailed complexity model for multiple-constant multiplication (MCM) has been derived and corresponding algorithms developed. It was shown that significant savings could be obtained using the proposed methodology.

Es6 Low-Complexity Digital Filters and Filter Banks

(Linnea Rosenbaum, student, and Håkan Johansson, supervisor)

Objectives: This project is concerned with digital filters and filter banks (FBs) which are frequently used in, e.g., digital communication, and speech, audio, and image processing applications. To focus is on the development of low-complexity filter and FB algorithms leading to implementations with low energy consumption. Of particular interest is the design and implementation of asymmetric and near-PR (Perfect Reconstruction) FBs. Asymmetric FBs are of interest in applications where it is important to minimize the complexity of either the analysis or the synthesis parts. One such example is communication systems consisting of a stationary unit and a mobile unit where it is crucial to minimize the power consumption in the mobile unit whereas one can afford a somewhat higher power consumption in the stationary unit. Another example is mixed discrete-time and digital FBs for analog-to-digital conversion where the analysis filters are discrete-time filters such as SC-filters. In this case it is essential to minimize the complexity of the SC-filters since these are much more difficult to implement with a high accuracy compared to digital filters. Near-PR FBs are used instead of PR FBs in order to reduce the complexity and power consumption.

Results: The main results are the introduction of several new different classes of cosine/sine modulated asymmetric and near-PR FBs as well as their design techniques. These new FBs have lower complexity than previous FBs. Further, an advantage of the proposed FBs and design techniques, over many previously existing techniques, is that the FBs can easily be designed to meet general specifications. The work has resulted in several publications at international and national conferences. One of the conference papers received the best paper award at the 2002 IEEE Nordic Signal Processing Symposium. One full-length paper has been submitted and two others are currently being prepared and will be submitted during 2005. Parts of this work were presented in Linnéas Licentiate Thesis "Contributions to low-complexity maximally decimated filter banks".

Es7 Estimation, synchronization, and equalization algorithms

(Mattias Olsson, student, and Håkan Johansson, supervisor)

Objectives: With the increasing need for high-performance signal processing and communication systems there is an increasing need for reliable and energy-efficient estimation, synchronization, and equalization algorithms for various purposes. This project is concerned with the development of such algorithms.

Results: One result of the project is a new carrier frequency-offset estimation algorithm that appears attractive compared to existing solutions. Another line of work is on delay estimation using special classes of digital filters. These delay estimation algorithms have the ability to estimate the delay with a very high precision for a broad class of signals which is difficult with other solutions. The algorithms have been successfully applied to estimate the static time-skew errors in time-interleaved ADCs. Measurements show that an overall ADC with performance beyond state-of-the art is obtained. The work has resulted in four publications at international and national conferences, and two additional papers that have been submitted. The results will be incorporated in Mattias Olsson Thesis to be presented during spring 2006.

Es8 Low Power Algorithm Design and Implementation

(Weidong Li, Anton Blad, Jonas Carlsson, PhD students, Oscar Gustafsson, Kent Palmkvist, co-supervisors, Lars Wanhammar, supervisor)

Objective: Low power design became crucial in the integrated circuit design. In portable applications, power consumption has long been one of the main constraints. In the high performance applications, low power techniques become more important due to the increasing cost for cooling and packaging. Besides those factors, the increasing power consumption has resulted in higher on-chip temperature, which in turn reduces the reliability. Therefore, low power and energy efficient techniques are important and must be used in current and future integrated circuits. The selected algorithm determines the overall number of operations per second. However, the operation scheduling and mapping to optimal hardware architecture determines the workdays for computation units and their power consumption as well as the communication requirements. Furthermore, the recursive loops in the algorithms significantly constrain the scheduling. These factors dramatically affect the power consumption and energy efficiency. Hitherto the power optimization techniques has essentially focused on a static view of the hardware resources, i.e., reduction of the switched capacitance, exploiting excess speed for power supply voltage reduction, gated clocks, etc. We aim to in this project also include the data dependencies in the analysis and synthesis of power efficient algorithms. For example, the interwire capacitance plays an important role in deep micron CMOS circuits. This has the effect that the Hamming distance between successive bus words should be minimized, since the it is proportional to the switching activity and power consumed. Furthermore, the data that are processed in most of the subsystems/algorithms used in communication systems, e.g., WLAN, are regular and reasonably well behaved. Hence, there exists a significant potential for reduction in the power consumption, but tools and methods for analysis and synthesis need to be developed. The aim for the project is to develop low power analysis and design methods for typical DSP algorithms and matching hardware structures.

Results: In the project several digital signal processing algorithms have been implemented using globally asynchronous, locally synchronous (GALS) techniques. Novel GALS wrappers for interconnection of blocks have also been proposed. Work on efficient implementation of FFT computations has temporarily been halted and instead we have focused on the problem of decoding low-density parity-check (LDPC) error correcting codes has been studied. A novel decoding strategy called early decision decoding has been proposed for low power decoding. Implementation of decoders to validate the results is ongoing.

A Licentiate Thesis “Studies on Asynchronous Communication Ports for GALS Systems”, have been published in June 2005. A part of the physical layer of a wireless LAN has successfully been tested in an FPGA using several clock domains with asynchronous communication in between. Currently the design

flow for GALS is investigated with the purpose to let a synchronous designer be able to use GALS without knowledge about asynchronous circuits.

As a continuation of our cooperation with Nanyang Technological University, NTH, Singapore, since the ASEAN-EU University Network Programme (AUNP) now has now been completed, we have planned a joint low-power asynchronous processor project for hearing-aid applications together with Professor Chang, Joseph Sylvesters, group at NTU. The project will start in early 2006.

Technology utilization

High speed interfaces (Jerzy Dabrowski)

Ek2 High Speed Off-Chip Communication

(Henrik Fredriksson, PhD student, and Christer Svensson, supervisor).

Objective: High datarate off-chip communication is often limited by reflections and other problems in the channel (circuit boards, contacts, etc). This is particularly true for buses with drops and stubs, like for example memory buses. The objective with this project is to demonstrate very high datarates (multi Gb/s) on memory buses on circuit boards, by utilizing adaptive equalizers and/or predistorters in the communicating chips.

Results: A concept for fulfilling the objective has been developed and verified in Matlab. One chip was been designed, fabricated and measured. This chip includes a complete decision feedback equalizer (DFE), with automatic blind coefficient update, aimed for 3Gb/s datarate. Most of the functionality was tested to 2Gb/s but some parts did not work at full speed. A new, improved, chip is under development, possibly also including some more functionality.

Degree of success: We have demonstrated the feasibility of using a DFE for improving the data rate on memory buses on a circuit board.

Ek5 Wide-band or tunable low noise RF amplifiers

(Stefan Andersson, PhD student, and Christer Svensson, supervisor).

Objective: A present trend is to make RF frontends more flexible, for example by having them covering several frequency bands. We aim at developing low noise amplifiers (LNA's) for such applications, that is LNA's which either have a very large bandwidth (covering several bands) or are tunable (can be tuned to a broad range of frequencies). We will use both bipolar and MOS technologies, thus facilitating a comparison between the two.

Results: A new concept for an inductorless, tunable LNA has been suggested and evaluated. Several amplifiers has been designed and fabricated, in 0.8μm CMOS, 0.18μm CMOS and 0.18μm BiCMOS. These amplifiers are aimed for 900MHz tunable, 2-6GHz wideband, and 2-6GHz tunable. Some measurements have been performed to date, but measurements are not finished. The project is closely related to the Soctrix demonstrator done at Acreo.

Degree of success: Results looks very promising, a broadband LNA with <5dB experimental noise figure for 2-6GHz and a tunable LNA covering 0.75-3GHz with 5dB noise figure has been experimentally demonstrated.

Ek11 RF frontend design for Software defined radio

(Stefan Andersson, Ph.D. student, Jerzy Dabrowski and Christer Svensson, supervisors)

Objective: Software defined radio (SDR) is a new concept catching large interest. It will need much very flexible RF frontend to become a reality. This research is aimed for creating such flexible RF frontends, based on RF sampling and discrete time filtering and decimation.

Result: A first implementation of a sampling solution has been developed, implemented and implemented. An experimental chip aimed at carrier frequencies up to 2.4GHz and bandwidths up to 20MHz was

successfully demonstrated and published in JSSC 2005. A second solution, based on a new, improved filter is under development and will be implemented in a 0.13µm CMOS process.

Degree of success: The sampling RF frontend published by us has rendered us very good visibility in Europe.

AD and DA converters (Mark Vesterbacka)

Es2 Reduction of substrate noise in mixed-signal circuits.

(Erik Backenius, PhD student and Mark Vesterbacka, supervisor)

Objectives: Major issues in large single-chip systems are the use of a common substrate for the analog and digital circuits, and the use of low-cost digital CMOS processes. There will also be more digital signal processing circuits within the mixed-signal circuits in the future. This project aims at alleviating the problems incurred in the analog domain by using digital circuit techniques and algorithms. In particular, we have targeted the problem associated with the use of a common substrate for analog and digital circuits. Sharing of the substrate causes the digital circuit noise to be propagated in the substrate and power supply lines to the sensitive analog circuits, thereby degrading their performance.

Results: The noise transfer mechanism in mixed-signal systems has been studied by modeling of the substrate using the finite element method. The developed model is valid up to a frequency of a few GHz, and it shows that high frequency components are significantly less attenuated in the substrate compared to low frequency components. This result agrees well with earlier research. A noise reduction strategy has been proposed. A special clock buffer and register circuit allow us to control the rise and fall time of the digital clock. This feature is used to reduce the high frequency content of the clock, leaving low frequency noise components that are easier to dampen. Another important property of the approach is that the clock buffer size can be decreased, which is beneficial for reducing the SSN. A test chip has been designed and the feasibility of the proposed noise reduction strategy has been demonstrated. In another test chip that currently is measured, a proposed on-chip measurement circuit has been implemented for measuring noise in the power supply lines.

Es3 High performance ADCs implemented in SOI technology

(Erik Säll, PhD student and Mark Vesterbacka, supervisor)

Objectives: The silicon on insulator (SOI) technology has until now mostly been used for RF and digital applications. Compared with traditional bulk technology, the parasitic capacitance is reduced, the current drive is higher, and the substrate coupling is reduced. Hence, using SOI also for analog and mixed-signal applications is very interesting. However, due to additional unwanted effects compared with bulk technology it is necessary to investigate how to modify existing circuits to make them usable for SOI, or invent new circuits that are more suitable for SOI. The main goal with this project is to design and implement analog building blocks that can be used for the evaluation of SOI. We chose to focus on the ADC, since it is a crucial component in most designs, and it includes design of several common analog building blocks.

Results: A 6-bit 1 GHz low power flash ADC has been designed and implemented that targets, e.g., read channel and ultra wideband communication applications. Five test chips have been manufactured in a 0.13 um SOI technology and is currently measured. They implement individual building blocks and test different techniques in the ADC. One test chip aims at evaluating a new DEM technique (compare with project Es1 where the DEM target is DAC) that we have recently proposed. Two test chips are full speed converters that use different digital decoders. We have proposed one of the decoders and expect it to be more efficient in terms of latency and power consumption compared to the other, conventional circuit.

High performance, low power circuit techniques (Atila Alvandpour)

Ek7 Low Power Multi-GHz Clocking

(Martin Hansson, Behzad Mesgarzadeh, Ph.D. students, Atila Alvandpour, supervisor)

Objectives: Power consumption has been identified as one the most serious challenges for future microprocessors and other advanced VLSI chips. It has been shown that up to 50% of the total chip power consumption in today's microprocessors is due to driving the clocked devices. Consequently, any significant reduction in clock power consumption would be considered as a major progress enabling the future high performance VLSI products. We are doing a comprehensive and systematic research on low power, Multi-GHz clocking techniques. Conventional high performance clocking techniques are mature and robust. However they are still based on a relatively rigid and traditional philosophy, which enforces a power hungry combination of dense clock distribution, full swing clock signals with fast edge rates, and large number of clocking elements, leaving almost no room for low power. Our circuit research targets radically lower power and energy efficient clocking techniques with the following approach:

- Research and development of a multi-GHz, energy-recyclable and/or low swing clock delivery technique.
- Research and development of low power and high performance flip-flops and latches supporting the proposed generated clock waveform and/or the conventional clock signals.
- Research and development of a general high performance circuit design methodology utilizing the proposed clocking technique.

Results: Several studies have been completed and promising low power circuit techniques have been developed or are under development through the following sub-tasks.

1- A low clock-load, high performance flip-flop has been developed and it was presented at IEEE SOCC conference, Santa Clara. Also, the flip-flop is included in a test-chip to be measured soon.
2- A comparative study on impact of sinusoidal clock signals on power and performance of conventional flip-flops has been completed. The results of this sub-task have been very useful for development of new flip-flops optimized to be directly driven by resonant LC-tank clock generators.
3- A study and comparison of On-Chip LC Oscillators for Energy Recovery Clocking has been completed. The study has been used for development of new LC-tank resonant clock generators.
4- Feasibility study and design of a complete resonant clocking technique including the LC-tank, clock distribution network, and the clock load. The result of this work has been useful for further development of the main project.
5- Development and design of the first demonstrator (test chip) for the proposed low power resonant clocking technique.
6- Completed measurement of the test chip in a 130nm CMOS technology. Where, we are now proud to report a successful experiment of 1.56 GHz on-chip LC-tank resonant clock oscillator which directly distributes and drives 2x896 flip flops, without intermediate buffers. Detailed power measurements of the test-chip in 130 nm CMOS show that the resonant clocking network consumes 2.3X lower power compared to the conventional clocking in the same chip. To our knowledge, this work reports so far the fastest on-chip LC-tank energy-recovery clocking without any intermediate clock buffers, and the first successful experiment studying the impact of the resonant clocking on flip-flops and data paths power consumption. The measurement result will be submitted for publication.

Ek8 Embedded Memories

(Stefan Andersson, Sreedhar Natarajan, Ph.D. students, Ingvar Carlsson, MS student, Atila Alvandpour, supervisor)

Objective: There is an increasingly large demand for embedded memories, which occupy a large portion of the chip area, and consume a significant portion of chip power consumption. In this project, we target low power, low-leakage, low-voltage, and high-density circuit techniques for embedded memories.

Result: Previously we reported the development and design of an embedded high density 128Kb SRAM memory utilizing a 5-Transistor single bitline memory cell in a standard 0.18µm CMOS technology. Post-layout simulations showed promising results, and the simulation results was accepted and presented at ESSCIRC 2004. The test chip in 0.18µm CMOS was taped out. Based on a complete chip measurement, we are now pleased to report a high density, fully static 128Kb on-chip cache utilizing 5-transistor (5T) single-bitline memory cells in a standard 0.18µm CMOS technology. Compared to a 128Kb 6T SRAM in the same process, the 5T SRAM has 23% smaller area and 4X lower bitline leakage. Correct and robust write operation across the process corners has been ensured by an intermediate bitline precharge voltage and the corresponding memory cell sizing. Despite the single bitline, a differential sensing scheme results in a comparable read-time (360ps, at 1.8V) and a 6T-compatible read/write scheme without requiring any extra signal or access to any additional cell nodes. The operation of every single memory cell has been successfully tested over a supply voltage range of 1V-to-1.8V.

Ek9 System On-chip Synchronization and Communication Techniques

(Behzad Mesgarzaedh, Peter Caputa, Ph.D. students, Christer Svensson, Atila Alvandpour, supervisors)

Objective: On-chip synchronization and communication are also major challenges for large and complex systems on-chip. We aim for low-cost, scalable, robust, and efficient techniques that significantly improve the on-chip timing issues. There currently several independent projects in this direction:

– On-chip Oscillators. This project targets on-chip clock generators and oscillators. We study the highly nonlinear behavior of these components, and we aim for accurate evaluation, characterization, and implementation of oscillators with robust oscillation, increased tune-ability, minimum jitter and phase noise.

Results: In addition to the comprehensive study of LC-tank oscillators for our low power, multi-GHz clocking (described in previous section), we are also developing analytical models and circuit techniques for injection locking techniques to reduce the jitter in oscillators. An analytical study of the injection locking for ring-oscillators has been completed. The work is accepted to be presented at ISCAS'05. Also, a test-chip is in progress.

– Synchronous Latency Insensitive Design. We have developed an efficient method to mitigate serious issues for system on-chip global communication without introducing asynchronous interfaces. During synthesis we replace fixed delays with synchronizing ports (elastic FIFOs) that absorb all link latencies and clock skews. The final design is a *Clock true model* independently of link delays and clock skews. Result: The proposed technique was accepted and presented at DAC'04. Two implementations of the technique have been completed including 1- an FPGA based design, which was successfully demonstrated, and 2- a test chip in 0.18µm CMOS, which was successfully demonstrated and presented at 1SSCC06.

Ek10 Low power, High performance Processor Building Blocks

(Sriram Vangal, Ph.D. student, Atila Alvandpour, supervisor)

Objective: Power consumption has been identified as one of the most serious challenges for future microprocessors, network, base-band, as well as signal processors. This project aims for new low power, high performance processor building blocks, where we focus on circuit, system, as well as architectures.

Result: We have developed and designed a six-port four-lane 57GB/s router core that features double-pumped crossbar channels and destination-aware channel drivers that dynamically configure based on the current flit destination. This enables 45% reduction in channel area, 23% overall chip area, and up to 3.8X reduction in peak channel power, depending on router traffic patterns. In a 150nm six-metal process, the 12.2mm^2 core contains 1.9 million transistors and operates at 1GHz at 1.2 V. The work has been submitted for publication.

Efficient design

Verification (Petru Eles)

Em4 Formal Verification of Embedded Systems in a Reuse Methodology

(Daniel Karlsson, PhD student; Petru Eles, Zebo Peng, supervisors)

Objectives: One of the important current trends in embedded systems design is towards a design process based on the reuse of pre-designed blocks. Such blocks can be both hardware and software components. With such a design process, also called ”interface based design”, the focus is on the interaction of components and, in particular, on interfaces, protocols and glue logic which interconnect independent blocks. Formal verification of embedded systems built in this way can be extremely complex and time consuming. However, it is reasonable to consider that the design of each individual reusable component has been verified before delivery and can be supposed to be correct. What remains to be verified is the correctness of the glue logic (hardware or software) and the way components interact. Such an approach can handle both the complexity aspects (by a divide and conquer strategy) and the lack of information concerning the internals of predefined components.

Results: We have developed a systematic synthesis flow and a verification methodology based on a formal representation using Petri Nets. The verification methodology avoids or reduces the effects of the inherent state explosion by taking advantage of the fact that the reusable components have already been verified and can be assumed to be correct. One of the basic ideas is to associate to each predefined component a set of predicates, expressing input/ output constraints. Such predicates are delivered together with the component. The final goal is to verify the correctness of the new system (in terms of functionality and timing), based on the predicates associated to reusable components and the Petri Net based model corresponding to the interface logic produced by the designer.

Testing (Zebo Peng)

Ek6 Testability-oriented Design Techniques for Mixed-Signal/ RF Integrated Circuits

(Rashad Ramzan, Ph.D. student, Xiaoqin Sheng, Muhannad Wasim, Noman Hai, MS students, Jerzy Dabrowski, supervisor).

Objectives: This project addresses testability of mixed analog-digital circuits. The goal is to demonstrate the applicability of DfT and BiST techniques to the design of mixedsignal/RF integrated circuits in CMOS technology. The relevant design methodologies will be developed and verified for design constraints and existing inherent limitations. Some principles that have already been borrowed from the digital domain and adopted in the analog domain need further study and application specific implementations. As a platform for the study on testability of mixed systems (AD/RF) a system on chip with both transmitter, receiver and digital parts will be used. The research program aims at structural tests by system architecture reconfiguration. In such cases the on-chip resources can be shared, e.g. analog output can be looped back to the analog input, thus facilitating built-in self-test. Integrated RF transceivers are considered a good demonstration platform for the project. Key problem areas are: design for test of RF blocks, analog/RF test pattern generation, fault modeling and fault simulation as a method to measure fault coverage for a given test set. An attempt will be made to develop cost effective test patterns (similar to the digital signature analysis) to limit hardware and test time. Pure digital testability issues fall beyond the scope of this research.

Results: The main results focus on test of RF transceivers, and they comprise the following: 1)Loopback BiST model with limited test circuitry suitable for different types of RF tests, exploiting abstraction levels. 2) Feasibility analysis of loopback BiST for different transceiver architectures. 3) Spot-defects modeling (typical of CMOS technology) based on noise and nonlinear analysis, circuit level perspective, fault simulation. 4) Techniques for sensitizing the RF test path for common faults in CMOS. 5) Comparative study of different tests applied to a RF transceiver (SER, EVM, IP3, gain). 6) Quantifying the masking effect of spot-faults by circuit tolerances, capturing the threshold of detectability for different tests. 7) Using mixed test (different tests) for enhanced fault coverage (SER/EVM, IP3, gain). 8) Design of test blocks for integration in CMOS technology. 9) Design of RF receiver front-end for enhanced test controllability (bypassing technique, test observation core).

Progress: During 2005 the main progress was on implementation side of the project. The most critical RF blocks of the demonstration platform have been designed using CMOS technology. To increase testability of the RF path, a bypassing technique has been implemented showing a reasonable tradeoff between test functionality and the chip performance in normal operation mode .

Em3 Hybrid BIST Methodology for Complex Electronic Systems

(Zhiyuan He PhD student; Zebo Peng, Petru Eles, supervisors)

Objectives: This project focuses on system-level test problems and the development of tools to provide test solutions for system-on-chip (SoC) designs. The test problems can be solved individually for each testable unit in the SoC. However, locally optimized solutions for each testable unit do not lead to a globally optimized solution. The basic problem for a test designer is to design test sets for each testable unit and to organize them in such a way that the global systems test cost is minimized. A technique for SoC testing that has gained increasing acceptance is BIST, which based on on-chip pseudo-random pattern generation. However, it is difficult and time consuming to perform high-quality self-test with only on-chip test resources. An interesting solution is to combine pseudo-random self-test patterns with deterministic test patterns, applied from an external tester or on-chip memory. Such a hybrid-BIST approach requires careful scheduling of the test sets in order to keep the test application time, power consumption, and the temperature under control.

Results: We have developed a method for optimizing the hybrid BIST approach. It enables us to find the most cost-effective combination of the two test sets not only in terms of test time but also in terms of on-chip memory requirements. We have earlier demonstrated the efficiency of such an approach for individual cores, and now have developed techniques to apply the same principle also for complex systems with multiple cores. We have also developed algorithms to take the defect probabilities into account in order to improve the schedule's quality.

Em5 Testing System-On-Chips Using Functional Bus

(Anders Larsson, PhD student; Zebo Peng, Petru Eles, Erik Larsson, supervisors)

Objectives: The main purpose of this work is to develop a SOC testing method, which minimizes the area overhead, and eases the ability of applying scan test to the cores. In this project the focus will be on using the functional connections (functional bus), to transport the test data between cores, sources, and sinks. Reusing the functional bus to transport test data to the cores minimizes the area overhead and it also tests the bus itself at the same time.

Results: Several techniques have been developed to apply tests to several cores in a concurrent fashion, including using multiple buses, inserting test data buffers between a core and a bus, and broadcasting test data to several cores. We have implemented two set of algorithms, one based on exact procedures that always generate the optimal solutions, and the other using heuristics, to determine the size of the buffers, the schedule of the broadcasted tests, and the topologies of the buses, as well as the infra structure needed to perform the tests.

Em9 SoC Wrapper Design, TAM Configuration and Test Scheduling

(Erik Larsson, researcher).

Objectives: This project deals with several issues related to the testing of system-on-chip designs (SoC), including the design of wrappers for cores, the selection and configuration of the test access mechanism (TAM), and test scheduling under certain design constraints such as power, time and cost, as well as the integration of the test infrastructure design into the design flow.

Results: Several heuristics to perform core test scheduling in a system, taking into account test parallelism constraints like test resource sharing, power limitation, and precedence constraint have been developed. Since cores are burned on the same silicon die, one major problem in testing is their accessibility. Designers have to find solutions in order to bring the test vectors to core inputs and to propagate the test responses from the core outputs to the system outputs. For each core, an isolation ring (wrapper) is usually needed, and a Test Access Mechanism (TAM) should be used to provide the accessibility of the cores in the whole system. We have developed approaches to support the design of these structures, first at the IP level (wrapper) and then at the system level including the test schedule as an integrated issue. We have also developed techniques to consider testability together with core selection, in the earlier design phase.

Em10: Analysis and design of fault-tolerant embedded systems

(Viacheslav Izosimov, PhD student, Zebo Peng, Petru Eles, Paul Pop, supervisors)

Objectives: This project aims at the development of fault-tolerant techniques to deal mainly with transient faults. We know that hardware architecture solutions, such as MARS, TTA and XBW, rely on hardware replication to tolerate permanent faults. Such approaches can be used for tolerating transient faults as well, but they incur very large hardware cost, especially if the number of (transient) faults is larger. Therefore software solutions such as re-execution, replication, check-pointing can be much more efficient. This project studies the optimal deployment of such solutions in the context of embedded system design where

task and communication scheduling should be performed, taking into account deadlines as well as fault-tolerant requirements.

Results: We have developed an approach to the design optimization of fault-tolerant embedded systems for safety-critical applications. Processes are statically scheduled and communications are performed using the time-triggered protocol. We use process re-execution and replication for tolerating transient faults. Our design optimization approach decides the mapping of processes to processors and the assignment of fault-tolerant policies to processes such that transient faults are tolerated and the timing constraints of the application are satisfied. We present several heuristics which are able to find fault-tolerant implementations given a limited amount of resources.