Measurement Point Selection for In-Operation Wear-Out Monitoring

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Abstract - *In recent IC designs, the risk of early failure due to electromigration wear-out has increased due to reduced feature dimensions. To give a warning of impending failure, wear-out monitoring approaches have included delay measurement circuitry on-chip. Due to the high cost of delay measurement circuitry this paper presents a method to reduce the number of necessary measurement points. The proposed method is based on identification of wear-out sensitive interconnects and selects a small number of measurement points that can be used to observe the state of all the wear-out sensitive interconnects. The method is demonstrated on ISCAS85 benchmark ICs with encouraging results.*

I. Introduction

In the pursuit of faster, feature-richer and less power-consuming ICs, feature dimensions (transistor dimensions and interconnect width) are pushed further and further into the deep submicron region in each process generation. This is relevant in the context of electromigration, which is a wear-out process which may cause ICs to fail in operation. The thinner an interconnect is, the sooner it may fail [1]. Wear-out monitoring aims at predicting impending failure due to wear-out and give a timely warning. While electromigration has been a known failure mechanism in ICs since the first ICs in the 1960ies, the recent reductions in the cross-section area of interconnects have caused IC failure due to electromigration to become a significant issue [2]. The rate of interconnect wear-out was previously small in comparison with the interconnect cross-section area and the mean-time-to-failure ($MTTF$) was large in comparison with the expected period of use of the IC. With reduced cross-section area of interconnects and the same rate of interconnect wear-out, $MTTF$ has become short enough to impact the useful life-time of ICs.

Several studies [3], [4], [5], [6], [7], [8] have developed methods to predict the location of electromigration-induced damage in order to adapt the IC design and reduce the risk of IC failure due to electromigration. Other studies [9], [10], [11], [12], [13], [14] have proposed embedding wear-out monitors into the design to predict the time of failure. The typical approach to wear-out monitoring is to measure the delay through the combinatorial parts of the IC to observe propagation delay increase, which is indicative of wear-out. An obstacle to the introduction of embedded wear-out monitors is the cost in terms of the silicon area required for the monitors. Whether the monitors are based on additional latches on the IC's flip-flops, as suggested in [11], or based on actual delay measurement circuits, as in [13], the cost scales with the number of measurement points.

In this context, this paper suggests a method for enabling low-cost wear-out monitoring and thereby reduce the cost of predicting failure due to electromigration. The method selects a low number of measurement points such that measurements performed will cover the full set of interconnects that can be considered sensitive to electromigration based on the knowledge of electromigration presented in Section II. Previous approaches to wear-out monitoring are reviewed in Section III and the wear-out monitoring approach considered in this paper is described in Section IV. In the context of that approach, the set of measurement points is determined using the proposed method which is described in Section V. Further, Section VI presents encouraging results based on ISCAS85 benchmark circuits and Section VII concludes the paper.

II. Electromigration Background

The following will review the factors that influence the rate of wear-out due to electromigration.

The wear-out mechanism electromigration describes gradual movement of metal atoms when influenced by a current [8]. The movement is caused by high-momentum electrons that transfer some of their momentum to the metal atoms. Electromigration is only an issue in interconnects that are longer than a certain *Blech length* L, which is a function of the current density J (current I divided by interconnect cross-section area A), as explained in [15]. It should be noted that most interconnects are longer than the Blech length. The following discussion applies to interconnects that are longer than the Blech length.

Electromigration can cause voids to form in some segment of the interconnect, often a via or a contact. Because of the void, the (already small) cross-section area of the segment will be reduced, and this leads to increased resistance and consequently increased signal delay. With further wear-out, the void (and the resulting delay) will grow until the interconnect is broken and the void has developed into a full open defect. The effect is that ICs that are proved fault-free by manufacturing test fail in operation after an unexpectedly short time (which may be measured in months or years).

It has been reported in [8] that if the interconnect is narrow, this will reduce the electromigration effect. This is because of the grain structure of the material in the interconnect. Typically

an interconnect is not perfectly homogeneous as a crystal but is made up of grains. As voids tend to form where the grains meet, an interconnect which is as narrow as the typical grain size will reduce the probability for voids to form. However, as described in [5], voids can form also within grains and narrow interconnect cannot prevent wear-out due to electromigration altogether.

The rate of wear-out increases with the current density, because the higher the current density, the more frequent is the movement of metal atoms. In fact, the current density in interconnects during switching of logic states in CMOS ICs has been non-decreasing over the process generations. This is because supply voltage and interconnect cross-section area have historically scaled in similar rates. The result is an increase in wear-out rate and more importantly, the today's manufactured defect-free interconnects have a smaller nominal cross-section area than in the previous decade. Therefore, $MTTF$ as described by Black's equation [1] (Equation 1) has decreased. Here, A is the original cross-section area, E_a is the activation energy specific to the material, J is the current density and T is the temperature. Furthermore, k is the Boltzmann's constant and n is a scaling factor.

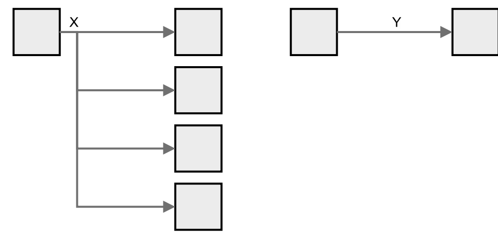
$$MTTF = A \cdot (J^{-n}) \cdot e^{\frac{E_a}{k \cdot T}} \quad (1)$$

From Black's equation (Equation 1), it can be seen that the rate of wear-out increases with increasing current density and increasing temperature as well as with constant current density and decreasing cross-section area. It should be noted that as the cross-section area A decreases, the resistance R of the wire increases as $R \propto A^{-1}$, which means that the current I decreases as $I \propto A$ (as can be seen by $I = V/R$ and $R \propto A^{-1}$), resulting in a constant current density $J = I/A$. Seen from another perspective, this means that for a given interconnect and a constant voltage across the interconnect, the rate of wear-out on the interconnect is constant, even though the cross-section area is gradually reduced as a result of wear-out.

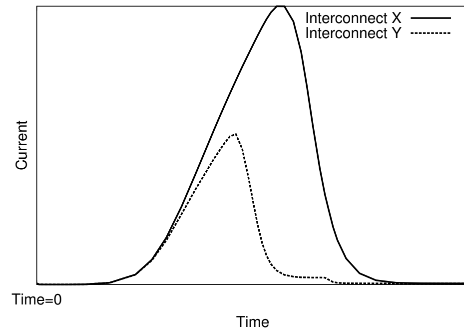
To mitigate electromigration, copper has been used to replace aluminum as material for metal interconnects, since copper is less susceptible to electromigration and has higher activation energy than aluminum [5]. However, the use of copper does not prevent electromigration altogether [5].

It should be noted that Black's equation (Equation 1) describes $MTTF$ under a constant flow of current. In fact, digital ICs in CMOS technology ideally has non-zero current only while switching between logic states. Therefore, the number of logic state switches that an interconnect has been subjected to influences its state of wear-out. This means that interconnects with high signal activity, i.e. where there are frequent switches of logic states, are particularly affected by electromigration.

The duration of current flow in each logic state switch has an impact on the wear-out accomplished. Figure 1 illustrates how an interconnect X with a fanout of four has a larger capacitive load than an interconnect Y with a fanout of one.



(a) Interconnect X and Interconnect Y



(b) Current waveforms

Fig. 1. Comparison of interconnects with high and low fanout

The interconnect X will be subjected to a higher current for a longer period of time. This is illustrated in Figure 1(b), where the currents through the driver of X and the driver of Y are shown for a logic switch initiated at Time=0. The reason behind the longer-lasting current through X is that it takes longer time to charge or discharge a large capacitor than a small capacitor with constant supply voltage.

To summarize the above, the interconnects which are likely to be worst affected by electromigration are longer than the Blech length, have a small cross-section area, are more than a grain size wide, are subjected to much signal activity (in terms of number of switches between logic states per time unit) and have a large fanout. Furthermore, interconnects in a hot-spot area of the IC will be worse affected than interconnects in cooler areas.

Based on the above, this paper will describe how a set of interconnects called Wear-out Sensitive Nets (WSNs) can be identified. The WSNs are the interconnects that are more susceptible to electromigration than other interconnects. Furthermore, the paper will propose a method for finding the appropriate minimal number of measurement points for on-line monitoring of the set of WSNs. The purpose is to reduce the cost of predicting failure due to electromigration.

III. Previous Work on Electromigration Wear-Out Monitoring

In known approaches to wear-out monitoring [9], [10], [16], [11], [12], [13], [14], some consider electromigration [9], some consider NBTI (Negative Bias Temperature Instability) [11], [12], [14], some gate oxide breakdown [9], [13] or some other or unspecified wear-out mechanism [16], [17]. Several of the known wear-out mechanisms have in common that

they affect the signal propagation delay through a circuit. Therefore, many wear-out monitoring approaches are based on observing delay or slack. It is inherently difficult to identify the wear-out mechanism that lead to delay increase, just based on delay measurements. Therefore, the known wear-out monitoring approaches react indiscriminate of the wear-out mechanism. Four main approaches can be listed as follows.

- Prognostic cells [9] are designed to fail due to wear-out before the functional parts of the IC. When a prognostic cell (a.k.a. canary circuit) fails, it is likely that the functional parts are also affected by wear-out, since they have operated under the same conditions. The approach with prognostic cells has the benefit that it can monitor wear-out without interrupting the functional processing of the IC. However, this can lead to a premature warning, since it is not known to what extent the functional parts are affected by wear-out.
- One type of wear-out monitors are based on regularly performed speed tests [10]. Reduction in system-wide slack indicates impending failure due to wear-out. In such approaches, the speed tests are performed at an interval, adjusted for sufficient sampling of the IC state for effective monitoring while ascertaining that the monitoring circuitry is active so infrequently that it does not wear-out before the functional parts of the IC [16]. During speed tests, the monitored parts of the IC must be in test mode. Therefore, the monitoring is scheduled for times in which the IC is idle. This approach of using speed tests cannot give relevant warning for wear-out on short paths for which the nominal delay is short in comparison with the clock period. Significant wear-out would have already occurred when detected.
- Another type of wear-out monitors are based on augmented flip-flops for checking a guard-band [11], [12]. An approach was described in [11] with an adjustable guard-band, which tracks the smallest slack over all the monitored flip-flops. Some reduction in slack is tolerated, and the information from the augmented flip-flops are used to compensate by adjusting the supply voltage, etc. When such mitigating efforts eventually become insufficient, a warning is given. It should be noted that this approach cannot monitor short paths.
- A third type of monitors employ explicit delay (or slack) measurements on selected combinatorial paths [13]. In a sequential circuit, the combinatorial parts receive their inputs from flip-flop outputs or the primary inputs, and their outputs are flip-flop inputs or primary outputs. This approach requires on-chip delay measurement circuitry, which can be a significant silicon area overhead. A low-overhead delay measurement circuit was presented in [18]. However, a typical use of such circuitry includes demultiplexing, which makes it possible to measure the delay at several outputs (several measurement points) with a single delay measurement circuit, albeit not simultaneously. The benefit of the approach with delay measurements is that also short paths can be monitored explicitly. It should be noted that delay measurements that target particular paths are performed in test-mode and require predetermined input vectors to set up the path and to trigger a signal transition on that path.

All of the four main approaches for wear-out monitoring detailed above could be applied to target electromigration wear-out. It should be noted that there is a trade-off between the monitoring capability and overhead, with explicit delay measurements being the approach with the highest overhead but with ability to target long and short paths alike.

In the context of the above, the work in this paper considers an approach (detailed in Section IV) with explicit delay measurements because that approach suits the aim to target interconnects that are particularly sensitive to electromigration wear-out and these interconnects may be found on short paths. The method presented in Section V describes how to keep down the cost of the delay measurement circuitry by identifying a small number of measurement points. For the wear-out mechanism NBTI, identification of sensitive circuitry has been done to aid wear-out monitoring, in [14], but this paper presents the first combination of identification of sensitive circuitry and wear-out monitoring for electromigration.

IV. Approach to Wear-Out Monitoring

To give a context to the main contribution of this paper, this section presents a conceptual wear-out monitoring approach that employs delay measurement. The main contribution of this paper is a method (Section V) to select a small number of measurement points to reduce the cost of the described wear-out monitoring approach compared to the straight-forward approach of considering each output of the monitored circuit as a measurement point.

As the current density remains constant during the wear-out process it can be expected that the delay will increase gradually as the cross-section area of the interconnect is reduced (see Section II). This observation can be exploited for wear-out monitoring. By regular, semi-periodic measurements of the time it takes for a signal to propagate through the circuit along a path that includes an interconnect, changes in that signal propagation delay can be attributed to wear-out. When the additional delay due to wear-out has increased beyond some value corresponding to severe wear-out, such as a slack margin or an absolute value set based on knowledge of the particular interconnect geometry, the wear-out monitor should give a warning to the operator or the maintenance personnel for the system containing the monitored IC. Since the delay is the same as the clock period minus the slack, measuring the slack is sufficient for calculating the delay. The process from measurement to warning is described in Figure 2.

The first step is marked by (1) in Figure 2. A given pair of input vectors cause a signal transition at the input at a time corresponding to the start of the functional clock period. The pair of input vectors also set up a propagation path (marked by thick arrows) so that the signal transition travels through a series of gates and interconnects to an output. The path in

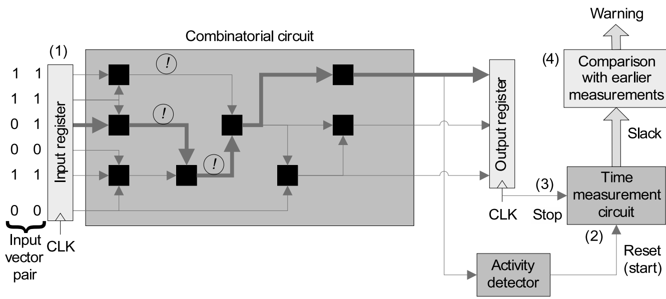


Fig. 2. Process from delay measurement to decision about giving warning

the example of Figure 2 includes two interconnects that are sensitive to electromigration wear-out. The identification of such interconnects is discussed in Section V.

As the second step in Figure 2, a measurement of the slack starts when the last transition occurs on the output.

In the third step, the slack measurement ends when the functional clock period ends. A slack measurement at the output *cover* all interconnects that are on the path. Since the delay is additive, any increase in delay (reduction in slack) can be caused by wear-out on some of or all of the covered interconnects. The wear-out monitor should give a warning for a significant increase in delay disrespective of if the wear-out occurs on only one of the interconnects or on all of them.

In the step marked (4) in Figure 2, the measured slack is compared against earlier measurements to determine if a warning should be given. If the comparison shows an increase in delay that is larger than some pre-determined value corresponding to significant wear-out, it is considered as significantly increased delay. It should be noted that other parameters than wear-out can affect the signal propagation delay. In particular, variations in temperature can temporarily affect the signal propagation delay through an IC [13]. One way to avoid giving false alarms when delay increase has been caused by temperature could be to give the warning only if the last few delay measurements indicate a consistent observation of significantly increased delay.

If no warning is given based on the measurement, the process continues by going back to step (1) to target another set of interconnects. When all considered interconnects have been covered or when a warning has been given, the delay monitoring process ends and is scheduled to restart at a later time. It is important that delay (or slack) measurements that target a particular interconnect are performed with the same sequence of input vectors each time. Otherwise differences between input vectors can cause variation in signal propagation delay. Furthermore, the delay measurements should be performed often enough to make it possible to give a warning before the wear-out results in functional faults.

The monitoring approach described above is based on explicit slack measurements, similar to the delay measurements in [13], adapted to the low overhead delay measurement circuit presented in [18]. The measurements are performed regularly, using pre-generated test vectors, while the monitored circuit is idle, at appropriate intervals to keep the monitors from wearing out before the monitored circuit, as in [16].

V. METHOD

The method for selecting a low number of delay measurement points to achieve a low-cost wear-out monitoring solution is divided in two phases, wear-out sensitive net (WSN) identification (Figure 3) and measurement point selection (Figure 4). A key idea in the method is to place delay measurement points on the outputs of the combinational parts of the IC that is to be equipped with wear-out monitoring capability. The delay observed at these outputs includes the increased delay from interconnects that are degraded due to electromigration. The method selects the appropriate set of outputs to equip with delay measurement points to target the wear-out sensitive nets.

The WSN identification phase is detailed in Figure 3. The steps *Signal Activity Calculation* and *WSN Identification* are specific to the presented method and are marked with a darker shade. The other steps, *Synthesis*, *Place and Route* and *Thermal Simulation*, correspond to off-the-shelf tools. For a design, described by a netlist, and a sample input sequence, the WSN identification step generates a set of WSNs and a synthesized netlist. These outputs from the WSN identification step will be used as inputs to the measurement point selection phase. As can be seen in Figure 3, the WSN identification phase proceeds with Synthesis to produce a synthesized netlist. The synthesized netlist is analyzed together with the sample input sequence to find the signal activity on each interconnect. This analysis can be implemented using a logic-level circuit simulator to identify the circuit state for each input vector. The time complexity of the analysis to find the signal activity is $O(n \cdot v)$ for n interconnects and v input vectors. For two consecutive circuit states A and B, each interconnect i has two logic states A_i and B_i. If A_i is different from B_i, an activity counter for the interconnect is incremented. The signal activity is the activity count divided by the length of the sample input sequence v. To identify the WSNs, the synthesized netlist is analyzed together with the signal activities for the interconnects. If an interconnect has a fanout above a certain user-specified limit $FanoutLimit$ and a signal activity above another user-specified limit $SignalActivityLimit$, then the interconnect is regarded as a WSN. The complexity of the task to identify the WSNs is dominated by the signal activity calculation with the overall time complexity of $O(n \cdot v)$ as discussed above.

The experiments presented in Section VI will show results based on a $SignalActivityLimit$ of 0.49 and a $FanoutLimit$ of two, as a proof-of-concept that it is possible to narrow down the number of targeted interconnects and for the targeted interconnects find a small number of measurement points. No experiments beyond what is presented have been performed. However, from Section II it can be subsumed that the identification of WSNs can be further refined by considering the Blech length and hot-spots. For such consideration, it is necessary to generate the layout by place-and-route of the synthesized netlist and thermal simulation using the sample

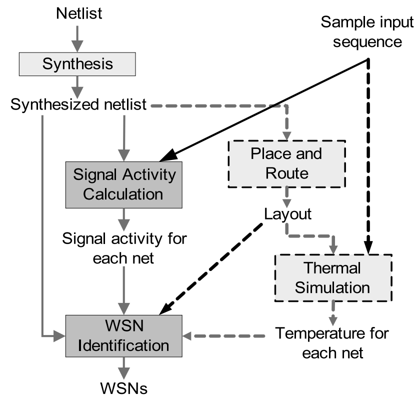


Fig. 3. Tool flow for WSN identification

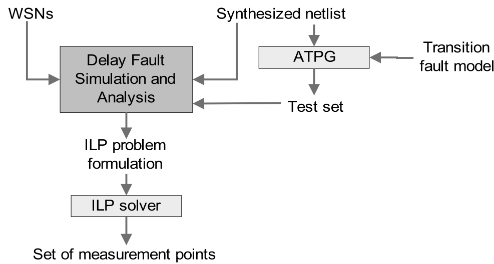


Fig. 4. Tool flow for measurement point selection

input sequence. The procedure is marked with dashed arrows in Figure 3. With consideration of Blech length and hot-spots, one could limit the selection of WSNs to interconnects that are longer than the Blech length and reach a temperature above some limit $ThermalLimit$. The proper adjustment of the $FanoutLimit$, $SignalActivityLimit$ and $ThermalLimit$ is outside the scope of this paper, but some appropriate values for $FanoutLimit$ and $SignalActivityLimit$ are discussed in Section VI. To demonstrate the method, the results in Section VI are based on a setup including only the interconnect signal activity and fanout for WSN identification (solid arrows and steps in Figure 3).

The measurement point selection phase is detailed in Figure 4. Here, the step *Delay Fault Simulation and Analysis* is specific to the proposed method and *ATPG* and *ILP solver* correspond to use of off-the-shelf tools. For the set of WSNs, the synthesized netlist and a transition fault test set generated by ATPG, an Integer Linear Programming (ILP) problem is formulated. A solver, such as LP_Solve [19], is applied on the ILP problem to arrive at a small set of delay measurement points for wear-out monitoring. The ILP problem is formulated

$$\text{minimize } \sum_{o \in Outputs} O_o$$
$$\forall_{w \in WSNs} \sum_{o \in Outputs} z_{w,o} \cdot O_o \geq 1$$
$$\forall_{o \in Outputs} 0 \leq O_o \leq 1$$

Fig. 5. ILP formulation

as shown in Figure 5. Here, O_o is a variable that is 1 if Output o is selected as a measurement point and 0 otherwise. Furthermore, $z_{w,o}$ is 1 if a delay fault on WSN w can be observed on Output o for any of the transition fault test vector pairs, and 0 otherwise. To obtain the $z_{w,o}$ values, fault simulation is performed using the transition fault test vector pairs with and without an inserted delay fault on each WSN. The set of outputs that depend on the existence of a delay fault are recorded in the $z_{w,o}$ values, as these outputs can be used to measure the propagation delay including the interconnect w where the delay fault was inserted, with the help of the considered test pattern pair. This fault simulation is a key task of the tool flow for measurement point selection as seen in Figure 4. The idea behind the ILP problem formulation is to find the outputs that can be used as measurement points for each WSN and then select the minimal set of outputs to target all WSNs. It should be noted that the minimal set of measurement points is selected with respect to a given set of transition fault test pattern pairs and a given set of WSNs.

VI. RESULTS

To demonstrate how the proposed measured output selection method can identify a small number of primary outputs for which delay measurements should be performed, experiments were performed on ISCAS85 benchmark circuits. The setup and the results of the experiments are described using Table I for detailing how wear-out sensitive nets (WSNs) are identified and Table II details how the WSNs are targeted by delay measurements on a number of outputs. In Table I, the four first columns show the name of the considered circuit, its number of gates, its number of outputs and its number of interconnects respectively. From the interconnects of each circuit, WSNs (right-most column) were identified based on the signal activity and the fanout. The signal activity was calculated based on a sequence of 1000 pseudo-random input vectors. Interconnects with signal activity higher than 0.49 transitions per clock cycle (fifth column) and a fanout of two or more (sixth column) were considered as WSNs. This means that the interconnects that are considered as WSNs change logic value about every other clock cycle and have more than the average capacitive load. As can be seen from Table I, less than half of the interconnects have such high signal activity and up to around 60% of the interconnects (in the case of c7552) can have such large fanout, and this depends on the circuit. It should be noted that the interconnects with high signal activity do not necessarily have large fanout, and this leads to a small number of WSNs.

Targeting the WSNs that are described in Table I, the experiment resulted in selection of a set of primary outputs as measured outputs as described in Table II. The first column shows the name of the considered circuit. To determine how the WSNs can be observed at the primary outputs, we used a set of transition fault test vector pairs, as described in Section V.

The number of test vector pairs are shown in the second column. The proposed method selected a small set of primary

TABLE I
FOUND WEAR-OUT SENSITIVE NETS IN ISCAS85 BENCHMARK DESIGNS

Circuit	Gates	Outputs	Inter-connects	Inter-connects with high activity	Inter-connects with large fanout	WSNs
C17	6	2	5	2	2	1
C432	160	7	173	42	61	2
C499	202	32	192	37	50	18
C880a	383	26	264	42	85	7
C1908	880	25	224	37	105	21
C2670	1269	140	337	112	113	34
C3540	1669	22	776	107	325	48
C7552	3513	108	844	381	503	186

TABLE II
RESULTS WITH ISCAS85 BENCHMARK DESIGNS

Circuit	Test vector pairs	Measured outputs	Ditto as fraction of outputs	Computation time
C17	6	1	50%	6s
C432	45	1	14.3%	3min
C499	80	2	6.3%	7min
C880a	35	5	19.2%	5min
C1908	67	1	4%	8min
C2670	55	8	5.7%	24min
C3540	135	4	18.1%	1h 20min
C7552	72	15	13.9%	4h

outputs that can be used to observe all the WSNs, and the number of selected primary outputs is shown in the third column. The fourth column shows the number of selected primary outputs as a fraction of the total number of primary outputs (see the third column of Table I). The right-most column shows the computation time. With respect to the computation time, it should be noted that the experiments were performed with in-house tools for calculating signal activity and for finding the primary outputs that can be used to target the WSNs. These tasks rely heavily on circuit simulation and fault simulation. With a state-of-the-art fault simulator to perform this task, computation time should be drastically reduced. Furthermore, computation time is not a very significant parameter, since measurement point selection is done during design time.

From the results in Table II it can be seen that compared to a wear-out monitoring approach that measures delay on all outputs of a combinational block of logic, the proposed approach can reduce the number of measured outputs by 50 (in the case of C17) to 96% (in the case of C1908). There is a relationship between the logic depth and the possible reductions in the number of measured outputs. For C17, the logic depth is 3 and for C1908, the logic depth can be 6 or above.

VII. CONCLUSION

This paper has considered the wear-out mechanism electromigration, which is a growing concern in modern semiconductor technologies, and presented a method for achieving low-cost wear-out monitoring by selecting a small number of measurement points for a delay measurement-based monitoring approach. The method is based on identification of wear-out sensitive interconnects and identification of outputs on which delay measurements can be performed to observe the wear-out state on the targeted interconnects. By solving an ILP problem a small set of outputs (measurement points) are selected such that delay measurements are possible including all targeted interconnects. The method was demonstrated on ISCAS85 benchmarks and reduction in the number of measurement points between 50% and 96% was observed compared to the straight-forward approach of measuring on all outputs.

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