COTEST/D4

Final Report on Project Results

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Related documents

- COTEST Technical Annex
- COTEST Report on Automatic Generation of Testbenches from System-level Descriptions (D2)
- COTEST Report on Early DfT Support (D3)

1. Introduction

The COTEST project aimed at assessing whether it is feasible and effective to take test issues into account early in the circuit design process, when a behavioral description of the circuit is available, only. The project focused on two main problems: generation of test sequences starting from behavioral descriptions and modification of behavioral descriptions to increase testability (Design for Testability). The project was based on an experimental approach exploiting a selected set of benchmark descriptions [1] to practically evaluate the feasibility and effectiveness of the considered techniques.

The experimental approach was selected mainly because it is the one with the highest chance of providing convincing results (especially when dealing with industry) but involved a significant effort to select suitable benchmarks, to set up an environment for evaluation, to devise and prototypically implement tools. During the project, the two partners successfully overcame this obstacle, and gathered a number of figures able to provide a detailed insight about the feasibility and effectiveness of available high-level test techniques.

This document contains the conclusions that can be drawn on top of the results gathered during the project, and better detailed in reports [2][3].

2. Test generation from behavioral-level descriptions

Any effort aiming at generating test sequences from high-level descriptions first need the availability of a suitable fault model.

During the project, an extensive experimental evaluation of the already proposed high-level fault models has been performed. The results can be summarized as follows:

- When *data-dominated circuits* are considered, the main issue concerns large combinational units possibly exploited during the synthesis process to implement high-level operators: since the structure of these units is not known, faults inside them can hardly be modeled at the high-level.
- When *control-dominated circuits* are considered, the main problem stems from modeling those faults belonging to the logic in charge of implementing the clocking and control strategy of the circuit, since this is implicit in any behavioral-level description.

Despite these limitations, experiments showed that it is possible to identify fault models providing a good correlation between high-level fault coverage and gate-level stuck-at fault coverage. In general, these fault models are not able to precisely foresee the gate-level fault coverage, but can be fruitfully exploited to rank sequences according to their testability value. Thanks to this property, these fault models are suitable to be used within automatic test generation algorithms.

Once a suitable fault model has been selected, the experimental results gathered with a relatively straightforward ATPG algorithm on the chosen benchmarks show that

generating sequences from high-level descriptions provides comparable results when compared with gate-level ATPG in terms of required CPU time, attained fault coverage and obtained test length. The advantages of high-level techniques seem more visible when dealing with data-dominated circuits than with control-dominated ones.

Since moving from higher to lover levels of abstractions means making more information available to the ATPG tool, the experiments showed that adopting a *hierarchical approach* can further increase the quality of the attained results.

It is important to note that, even when the results of test generation from high-level descriptions are only comparable with those of test generation from gate-level ones, the former is precious for the designer, since it provides early information about the testability of a circuit, thus avoiding expensive (in terms of cost and time) recycling through the synthesis step.

3. Early DfT support

One of the goals of this assessment project was evaluation of different test and DfT methodologies at higher level of abstraction. With our work we have experimentally demonstrated that it is feasible to reason about testability and to introduce DfT structures at early phases of design cycle. Particularly when there is some information available about the final architecture and we can incorporate structural information into the analysis. We have investigated possibilities of inserting self-test structures, as one of the dominating low-level DfT methodologies, in early phases of design flow and by introducing software based hybrid BIST architecture we have brought together hardware and software domains, making our approach flexible and very attractive for SoC solutions.

As it was demonstrated by the results produced by this project, working at high levels of abstraction allows to reduce the test generation effort by a factor ranging from 3 to 10, while keeping the same high quality. By inserting self-test structures our approach guarantees full (100%) testability, while reducing area overhead in terms of signature analyzers compared to the straightforward solution by 25% to 50%. This area overhead can further be reduced by using a hybrid BIST architecture, where some of the required test structures can be implemented in software. As it was demonstrated experimentally, with a hybrid BIST solution less than 50% of deterministic patterns and only a small fraction of pseudorandom vectors are needed, while the maximum achievable fault coverage is guaranteed.

4. Conclusions and Open Issues

The size and typology of the COTEST project clearly limited the amount of performed activities, e.g., in terms of considered benchmarks. However, the project produced a number of experimental figures allowing to better understand the advantages and limitations of currently available techniques for test activities performed at the behavioral level.

The following conclusions can be drawn from the project results:

- Generating sequences from high-level descriptions is feasible and the generated sequences can be effectively compared with those generated at gate level;
- Hierarchical test generation can effectively complement techniques working on high-level descriptions, only;
- DfT modifications at early phases of design cycle are feasible and should be investigated further.

We believe that the following issues are definitely worth of further investigations:

- Identification of more accurate fault models and test generation algorithms;
- Defect coverage (instead of stuck-at fault coverage) should be considered to assess the value of sequences and DfT structures devised at the high-level;
- The value of sequences generated from high-level descriptions is likely not to be limited to the test area, but could also concern validation and hardware design debug.

Finally, it is important to underline the value of any technique providing information about the testability of a circuit starting from high-level descriptions, since in this way the designer can possibly intervene early in the design phase, thus avoiding the cost of recycling through the synthesis step(s).

5. References

[1] M. Sonza Reorda, M. Violante, "Report on benchmark identification and planning of experiments to be performed", COTEST Report D1

[2] O. Goloubeva, M. Sonza Reorda, M. Violante, "Report on automatic generation of test benches from system-level descriptions," COTEST Report D2

[3] P. Eles, G. Jervan, Z. Peng, "Report on Early DfT Support," COTEST Report D3