Test Planning for 3D Stacked ICs with Through-Silicon Vias

Breeta SenGupta Urban Ingelsson Erik Larsson
Department of Computer and Information Science
Linköping University, SE-581 83 Linköping, Sweden
Email: {breeta.sengupta, urban.ingelsson, erik.larsson} (at) liu.se

***Abstract*—Test planning for core-based 3D stacked ICs with trough-silicon vias (3D TSV-SIC) is different from test planning for non-stacked ICs as the same test schedule cannot be applied both at wafer sort and package test. In this paper, we assume a test flow where each chip is tested individually at wafer sort and jointly at package test. We define cost functions and test planning optimization algorithms for non-stacked ICs and 3D TSV-SICs with two chips in the stack. We have implemented our techniques and experiments show significant reduction of test cost.**

***Index Terms*—Test Scheduling, 3D stacked IC, JTAG, Test Architecture, Through Silicon Via.**

I. Introduction

3D stacked ICs with trough-silicon vias (3D TSV-SICs) are emerging and have attracted a fair amount of research [1]–[6]. As the cost of test, which is highly related to test time and the additional design-for-test (DfT) hardware, accounts for a considerable part of the total manufacturing cost, it is important to develop a test plan minimizing the overall test cost. The testing of non-stacked ICs is well-defined; each IC is tested twice during the manufacturing process: during wafer sort, the bare chip (die) is tested, and during package test, the packaged IC is tested. For non-stacked ICs, the same tests are applied to the chip both during wafer sort and package test; hence, the same test schedule is used twice. However, for testing 3D TSV-SICs it is different. First, the test-flow is not well-defined. For 3D TSV-SICs, there are more test alternatives; testing can be performed on each individual IC, partial stacks, and/or the final stack. Second, as the number of tests are different in each of these steps, test schedules are to be developed for each step (each individual IC, partial stacks, and the final stack), which is the focus of this paper.

Much work on test scheduling for non-stacked ICs have been performed [7]–[10]. For example, Chou *et al.* proposed a test scheduling technique that organized the tests in sessions such that the test time is minimized while power constraints are met [8]. Muresan *et al.* [7] proposed a session-less test scheduling technique with the same optimization goal as Chou *et al.*. While, the test architecture is unclear in the approach by Muresan *et al.* [7], Iyengar *et al.* [11]–[13] and Marinissen *et al.* [14] proposed test scheduling techniques and test architecture optimization for IEEE 1500. However, no work has addressed test scheduling in an IEEE 1149.1 environment. An increasing amount of work address testing of 3D TSV-SICs [1]–[4], [15]–[17].

SenGupta *et al.* define the test flow in test cost is minimized while yield is maximized [15]. The scheme proposes that each individual IC is tested and then the complete stack is tested [15]. Marinissen *et al.* accounted for the variations in hardware required for various test schedules, although the overall test cost has not been optimized [16]. DfT hardware optimization has been addressed in [14], [18]–[20]. However, no work has addressed test scheduling. And, no work has defined test cost models and test planning algorithms that optimizes the overall test cost for 3D TSV- SICs in an IEEE 1149.1 environment.

In this paper, we assume a test flow as introduced by SenGupta *et al.* [15], an IEEE 1149.1 environment, and we define test cost functions and test planning optimization algorithms for non-stacked ICs followed by 3D TSV- SICs with two chips in the stack.

The rest of the paper is organized as follows. In Section III, the JTAG test architecture assumed in our work is detailed. The problem definition is in Section III. In Section IV, we show a motivational example on the test scheduling problem for 3D TSV-SICs. The proposed test scheduling techniques are in Section V. The paper is concluded with experimental results (Section VI) and conclusions (Section VII).

II. Test Architecture

The test architecture of a non-stacked IC, that assumed in this paper, is shown in Fig. 1. Here a chip is considered to consist of a number of cores that are accessed by an on-chip JTAG infrastructure [15]. The JTAG test access port (TAP) may have up to five terminals, namely Test Data Input (TDI), Test Data Output (TDO), Test Mode Select (TMS), Test Clock (TCK) and an optional Test Reset (TRST). In Fig. 1 only the TDI and TDO pins are shown, as the wafer sort interface terminals. Each core on a chip is accessed by the JTAG TAP via test data registers (TDRs). One TDR may be used to connect multiple cores on a single chip. In Fig. 1, the IC contains three cores: Core1, Core2 and Core3. Core1 and Core2 share a common TDR, while Core3 has an exclusive TDR. Only one TDR can be accessed at a time. Thus, if tests for more than one core of a chip are to be executed concurrently, in a session, as shown in Fig. 2, these cores are to be connected in series on the JTAG interface in one TDR. Since, Core1 and Core2 are tested in the same session as seen in Fig. 2, the two cores are connected to the JTAG TAP by the

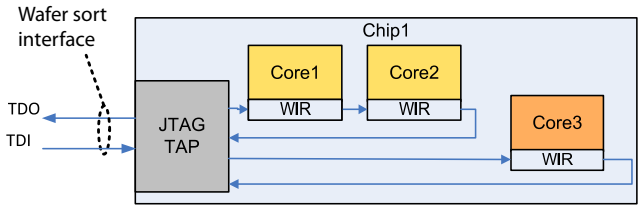

Fig. 1. Test architecture of a non-stacked chip with JTAG

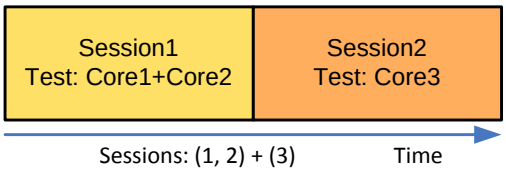

Fig. 2. Sessions formed by core tests

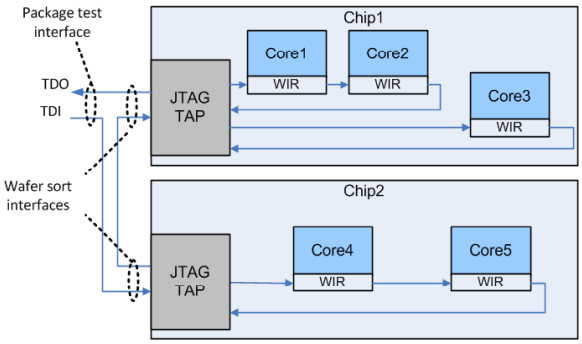

Fig. 3. Test architecture of 3D TSV-SIC with JTAG

same TDR, as seen in Fig. 1. Correspondingly, in Session2, only Core3 is tested, which is connected to the JTAG TAP by a single TDR.

During the package test of the 3D TSV-SIC, the TDO of the lower JTAG TAP in the stack serves as the TDI of the corresponding JTAG TAP of the chip on top of it. The TDO of the topmost chip is directed out via TSVs. The TDI of the lowermost chip and the TDO of the topmost chip serve as the package test interfaces as shown in Fig. 3. A session of tests from a chip can be performed concurrently with a session of tests from another chip by selecting the corresponding TDRs by the respective on-chip JTAG TAPs of to the two chips.

III. Problem Definition

In this section the test cost for non-stacked IC and 3D TSV-SIC with two chips in the stack are defined. The overall objective is a test plan with a minimal cost in terms of test application time (TAT) and hardware (number of TDRs), defined as:

$$Cost(TAT, TDR) = \alpha \cdot TAT + \beta \cdot TDR \quad (1)$$

where, α and β are constants set by the designer depending on the particular system.

A. Non-stacked IC

For a non-stacked IC with C cores, we assume for a core c_i, $1 \leq i \leq C$, having a scan chain of length l_i and requiring p_i test patterns. The test time for a core c_i is given by:

$$Time(c_i) = (l_i + 5) \cdot p_i + l_i \quad (2)$$

In the above equation, the 5 accounts for the number of clock cycles required by the JTAG for apply and capture.

A test schedule for the C cores consists of S sessions, where each core c_i belongs to an unique session S_j, $1 \leq j \leq S$. The number of cores that are tested in a session S_j is given by M_j. The test time T_j for a session S_j is denoted by:

$$T_j = \left(5 + \sum_{\forall k \in M_j} l_k\right) \cdot max(p_k) + \sum_{\forall k \in M_j} l_k \quad (3)$$

The overall test time for a test schedule is given as:

$$Time = \sum_{j=1}^{S} T_j \quad (4)$$

The hardware cost is directly related to the number of sessions as each session correspond to a TDR; hence, $TDR = S$.

In the case of non-stacked ICs, the same schedule is applied at wafer sort and at package test; hence, $TAT = 2 \cdot Time$.

The cost function in Eq.1 is in the case of non-stacked ICs given as:

$$\begin{aligned} Cost(TAT, TDR) &= \alpha \cdot TAT + \beta \cdot TDR \\ &= \alpha \cdot 2 \cdot Time + \beta \cdot S \end{aligned} \quad (5)$$

The problem is to find the test schedules for wafer sort and package test such that the overall TAT and number of sessions (TDRs) are minimized.

B. 3D TSV-SIC with two chips in the stack

For a 3D TSV-SIC design having a stack of two chips, Chip1 and Chip2, we assume that Chip1 and Chip2 have C_1 and C_2 cores, respectively. For each core c_{1i} in Chip1, $1 \leq i \leq C_1$, the length of the scan chain is l_{1i} and the number of patterns required is p_{1i}, while for each core c_{2j} in Chip2, $1 \leq j \leq C_2$, the length of the scan chain is l_{2j} and the number of patterns required is p_{2j}.

For wafer sort, Chip1 and Chip2 have test schedules with S_1 and S_2 sessions respectively. Each core c_{1i} belongs to an unique session S_{1m}, $1 \leq m \leq S_1$, and each core in Chip2 c_{2j} belongs to an unique session S_{2n}, $1 \leq n \leq S_2$. The number of cores that are tested in a session S_{1m} (S_{2n}) is given by M_{1m} (M_{2n}). The test time T_{1m} for a session S_{1m} session is denoted by:

$$T_{1m} = \left(5 + \sum_{\forall m \in M_{1m}} l_{1m}\right) \cdot max(p_{1m}) + \sum_{\forall m \in M_{1m}} l_{1m} \quad (6)$$

and the test time T_{2n} for a session S_{2n} session is denoted by:

$$T_{2n} = \left(5 + \sum_{\forall n \in M_{2n}} l_{2n}\right) \cdot max(p_{2n}) + \sum_{\forall n \in M_{2n}} l_{2n} \quad (7)$$

Given Eq.6, the test time for wafer sort for Chip1 is given as:

$$T_{1ws} = \sum_{m=1}^{S_1} T_{1m} \quad (8)$$

and given Eq.7, the test time for wafer sort for Chip2 is given as:

$$T_{2ws} = \sum_{n=1}^{S_2} T_{2n} \quad (9)$$

The total time taken for wafer sort is:

$$T_{ws} = T_{1ws} + T_{2ws} \quad (10)$$

For package test of Chip1 and Chip2 a test schedule with S_3 sessions is formed. Each core c_{1i} (c_{2j}) belongs to a unique session S_{3o}, $1 \leq o \leq S_3$. The number of cores that are tested in a session S_{3o} is given by M_{3o}. The test time T_{3o} for a session S_{3o} is denoted by:

$$T_{3o} = \left(5 + \sum_{\forall o \in M_{3o}} (l_{1o} + l_{2o})\right) \cdot max(p_{1o}, p_{2o}) + \sum_{\forall o \in M_{3o}} (l_{1o} + l_{2o}) \quad (11)$$

Given Eq.11, the test time for package test for Chip1 and Chip2 is given as:

$$T_{pt} = \sum_{o=1}^{S_3} T_{3o} \quad (12)$$

The hardware cost is directly related to the number of sessions as each session corresponds to a TDR; hence, the number of TDRs for package test is equal to S_3.

The TAT can be given by

$$TAT_{2chip} = T_{1ws} + T_{2ws} + T_{pt} \quad (13)$$

The total hardware cost is given as:

$$TDR = S_1 + S_2 + S_3 \quad (14)$$

The overall test cost can be expressed by the following equation:

TABLE I
GIVEN L, P VALUES FOR EACH CORE OF THE 3D TSV-SIC

	Chip 1			Chip 2	
	Core1	**Core2**	**Core3**	**Core4**	**Core5**
Scan chain length	50	40	30	20	10
Patterns required	50	40	30	20	10

$$\begin{aligned} Cost_{2chip}(TAT, TDR) &= \alpha \cdot TAT + \beta \cdot TDR \\ &= \alpha \cdot TAT_{2chip} + \beta \cdot (S_1 + S_2 + S_3) \end{aligned} \quad (15)$$

The problem is to find the test schedules for wafer sort of Chip1, wafer sort of Chip2, and package test for jointly testing of Chip1 and Chip2 such that the overall TAT and number of sessions (TDRs) are minimized.

IV. MOTIVATIONAL EXAMPLE

Here we present an example to demonstrate the problem of test scheduling to minimize the overall cost, defined by Eq.1. Given is a 3D TSV-SIC with two chips in the stack, illustrated in Fig. 3.

Table I lists the values of the scan chain length and the number of patterens required for each core of the 3D TSV-SIC with two chips, as shown in Fig. 3. The total test time for wafer sort, T_{ws}, and package test, T_{pt}, for the configuration shown, i.e., Core1 and Core2 with a common TDR, forming session S_1, Core3 forming session S_2, Core4: session S_3 and Core5: session S_4:

$$T_{ws} = T_{1+2} + T_3 + T_{4+5} = 6250 \; time \; units \; (t.u.) \quad (16)$$

Performing the tests in the same order on package test as in wafer sort would result in this case

$$T_{ws} = T_{pt} \quad (17)$$

Therefore the total test time becomes,

$$T = T_{ws} + T_{pt} = 6250 + 6250 = 12500 \; t.u. \quad (18)$$

Similarly, considering separate TDRs for all five cores would give, $T = 11600 \; t.u.$ But, it results in more sessions, thus an increased hardware cost.

The minimum number of sessions is obtained when during wafer sort Core1, Core2 and Core3 are in S_1 and Core4 and Core5 are in S_2, while during package test all five cores are in the same session. The total time leads to $T = 13640 \; t.u.$, which is much higher than the alternative distribution of sessions discussed above, although, in this case, the hardware requirement is minimum.

But during the package test, if the test of Core3 is performed along with Core4 and Core5, instead of Core1 and Core2, we find, in Table II, that the total test time is reduced to $T = 12780 \; t.u.$ It must be noted that this alternative demands fewer TDRs as compared to the first alternative where the five cores were tested in five different sessions during both wafer sort and

TABLE II
TEST SESSION ALTERNATIVES (WITH ALTERNATIVE 2 AS BASELINE)

Cases	**Wafer Sort** (T_{ws})				**Package Test** (T_{pt})		**Total Time**	**No. of TDRs**
	Chip 1		**Chip 2**				$t.u.$ (% incr.)	orig (% decr)
	Core Tests in Sessions	Time	Cores Test in Sessions	Time	Cores Test in Sessions	Time	$T_{ws} + T_{pt}$	
1	(1, 2) + (3)	5600	(4) + (5)	560	(1, 2) + (3) + (4) + (5)	6160	12320	4
2	(1) + (2) + (3)	5240	(4) + (5)	560	(1) + (2) + (3) + (4) + (5)	5800	11600	5
3	(1, 2, 3)	6170	(4, 5)	650	(1, 2, 3) + (4, 5)	6820	13640	2
4	(1, 2) + (3)	5600	(4, 5)	650	(1, 2) + (3) + (4, 5)	6250	12500	3
5	(1, 2) + (3)	5600	(4, 5)	650	(1, 2) + (3, 4, 5)	6530	12780	3

final test. On the other hand, this alternative requires lower test time as compared to the alternative where all cores of a chip are tested in the same session during wafer sort and there is only one session during package test.

Therefore, from the above studies on the distribution of TDRs in a 3D TSV-SIC it was seen that the test time can be reduced by increasing the number of TDRs, thereby increasing the number of sessions. Although, an increased number of sessions imply increased hardware cost. Hence, in this paper, we try to obtain a trade-off between the hardware cost and the test time in order to give the minimum total effective cost in terms of hardware cost and test time.

V. PROPOSED APPROACHES

In this section we propose three algorithms, for non-stacked IC, 3D TSV-SIC with two chips in the stack and 3D TSV-SICs with any number of chips in the stack, to arrive at a test plan which requires minimal overall test cost, in terms of TAT and the number of TDR, as defined in Eq.1.

A. Non-stacked IC

By the following steps of the algorithm we arrive at the reduced cost for non-stacked ICs.

- Given is the length of the scan chains l_i and the number of patterns required p_i of a list of C cores c_i, $1 \leq i \leq C$, in a chip. The list of cores, is sorted in descending order of the number of patterns required.
- The constants of the cost function defined by Eq.1, α and β are also provided.
- Initially, TAT is set equal to the test time of core c_1.
- The number of sessions, S is initially set equal to one. The first session, S_1, in the test schedule contains the test of core c_1. Core c_1 is then removed from the sorted list.
- Each core c_i, remaining in the sorted list, is descended in the following way:
  The increase in TAT for each core c_i is calculated by including it in all existing sessions. If the cost of a single TDR is less than the cost incurred by including the core test in any of the existing sessions due to the increased test time, the core test forms a new session.
  Once the core is assigned a session, it is excluded from the sorted list.
- The test plan is achieved when test of each core c_i, $1 \leq i \leq C$, has been assigned its respective session S_j.

TABLE IV
REDUCTION IN TAT FOR 3D TSV-SICS

Design nos.	**Cost Naive Approach**	**Cost Reduced**	**Percentage Reduction**
p22810, p93791	2584642	1951685	24.49
p93791, g1023	2006166	1292321	35.58
g1023, d695	1313282	737453	43.85
d695, h953	1045439	727092	30.45
h953, d281	2325887	599437	74.23

B. 3D TSV-SIC with two chips in the stack

The wafer sort test schedules for the two chips forming the 3D TSV-SIC, Chip1 and Chip2 are obtained by applying the algorithm for test scheduling of non-stacked ICs. The test planning algorithm for package test is discussed below:

- Given is the list of the test time taken by S_1 sessions of Chip1 and S_2 sessions of Chip2, denoted by T_{1m} and T_{2n} respectively.
  The lists of sessions of Chip1 and Chip2, S_{1m} and S_{2n}, are sorted in descending order of their test times, T_{1m} and T_{2n}.
- The test schedule for the package test is obtained by simultaneously initiating the sessions S_{1m} and S_{2n} for all $m = n$. The total number of sessions during package test is S_1 if $S_1 > S_2$, and S_2 otherwise.
- The reduction in test time for each new session formed during package test of the two chip 3D TSV-SIC is the test time of the session S_{1m}, if $S_{1m} < S_{2n}$ and S_{2n} otherwise.
  The sum of the reduction in test time over all the sessions formed during package test gives the overall reduction in the TAT.

VI. EXPERIMENTAL RESULTS

In this section we illustrate the benefits of the proposed approach for non-stacked ICs and 3D TSV-SICs with two chips in the stack.

Experiments have been performed on the six ITC'02 benchmark system on chip (SOC) designs mentioned below:

p22810, p93791, g1023, d695, h953 and d281.

The following assumptions were made when constructing 3D TSV-SICs from the non-stacked SOC benchmarks :

- The modules in the benchmark SOC designs are projected as cores in a non-stacked IC

TABLE III
TAT AND TDR FOR NON-STACKED IC

No.	Design	Minimal Test Cost			Cost with Minimum TAT Maximum TDR (= No. of cores)				Cost with Maximum TAT Minimum TDR (= 1)			
	Cost	TAT	TDR	Cost	TAT	TDR	Cost	Inc.(%)	TAT	TDR	Cost	Inc.(%)
1	**p22810**	501490	7	534250	474489	22	577449	8.1	2022377	1	2027057	279.4
2	**p93791**	614233	4	633701	589394	13	652665	3.0	1990806	1	1995673	214.9
3	**g1023**	46885	4	51813	42429	12	57213	10.4	137727	1	138959	168.2
4	**d695**	35757	4	40689	34331	8	44195	8.6	80369	1	81602	100.6
5	**h953**	271381	2	305483	230771	7	350128	14.6	418607	1	435658	42.6
6	**d281**	117946	2	144992	97310	5	164925	13.8	186458	1	199981	37.9

- All scan elements (inputs, outputs, and scan cells) at a core are connected to a single scan-chain
- 3D TSV-SICs are constructed by vertically stacking any number of the non-stacked designs
- The constant α in Eq.1 for all designs is considered to be one
- The constant β in Eq.1 for all designs is calculated by dividing the test time of the first core in the sorted list, $Time(c_1)$, by the number of cores, C.

A. Non-stacked IC

Table III compares the minimized overall cost for non-stacked ICs to the overall cost when the test time cost is minimal and to the overall cost when the cost of hardware is minimum, $i.e.$, there is only one TDR.

In Table III, each row corresponds to a SOC benchmark design, which is shown in the second column. The costs of three different test schedules are compared in the following three groups of columns. The first group of three columns shows the minimal test cost of the respective designs as obtained by the algorithm proposed in Section V. Next is the cost incurred when the TAT is minimum; in other words the hardware cost is maximum, with the number of TDRs equal to the number of cores in the IC. The last column in the group of four columns evaluates the increase in the test cost wrt the minimal test cost. The rightmost group of four columns shows the test cost when all cores share a common TDR, thereby maximizing TAT. In Table III, it can be seen that the maximum reduction in cost wrt minimized TAT is up to 15% for h953 and wrt minimized number of TDRs is up to 280% for p22810.

B. 3D TSV-SIC with two chips in the stack

In Table IV, the package test cost for various 3D TSV-SIC designs made by stacking the six benchmark designs in Table III are shown. The first column shows the benchmark designs that have been used to make the stack. The second column lists the minimized test cost obtained by summing up the test times of each design forming the stack, corresponding to the minimal cost, as obtained in Table III. The next column shows the reduced test cost by applying the algorithm proposed in Section V. In the rightmost column, the relative reduction in the test cost is evaluated. We can see that the test cost can reduce up to 74%, when chips h953 and d281 are stacked.

VII. CONCLUSION

In this paper, we define test cost as a function of TAT and the number of TDRs for non-stacked ICs and 3D TSV-SIC with two chips in the stack. The test cost is minimized by co-optimizing TAT and the number of TDRs. We propose an algorithm for scheduling tests, which addresses the following problems:

1) For a non-stacked IC, in an IEEE 1149.1 environment, where the same test schedule is applied during wafer sort and package tests, the tests of all the cores are grouped in sessions such that the cost is minimized by co-optimizing the TAT and the number of TDRs required. We find that the cost can increase by 280%, when either one of the variables are minimized.
2) For a 3D TSV-SIC, having two chips, each chip is tested individually during wafer sort and jointly during package test. The cost is minimized by forming sessions from different chips concurrently during the package test. Results show that by applying the algorithm, the test time can be reduced by up to 74%.

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