A Hybrid BIST Architecture and its Optimization for SoC Testing

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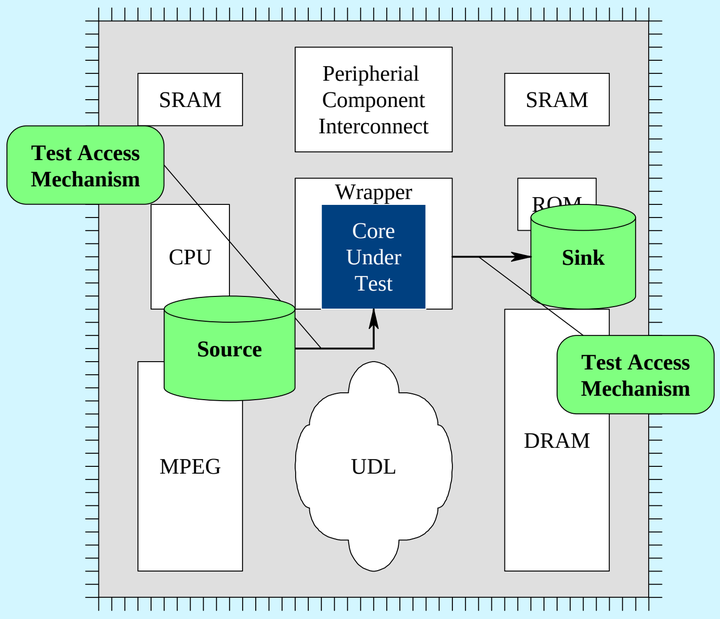
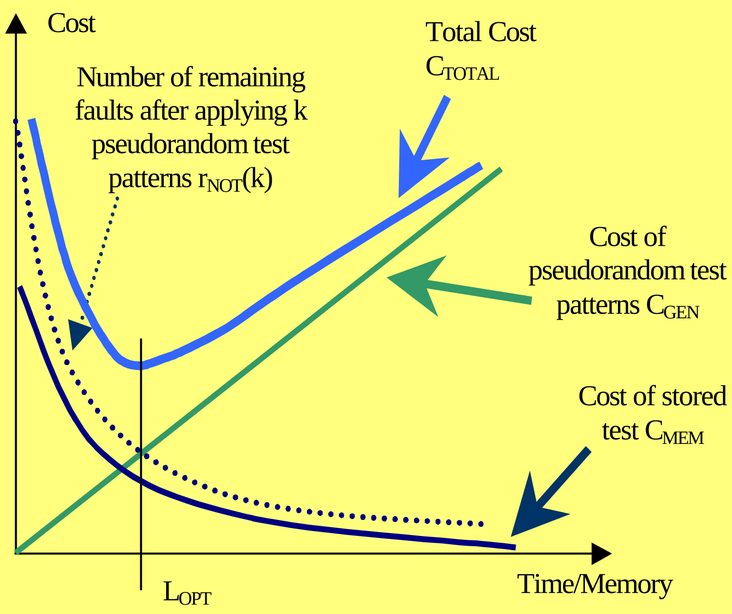
Overview

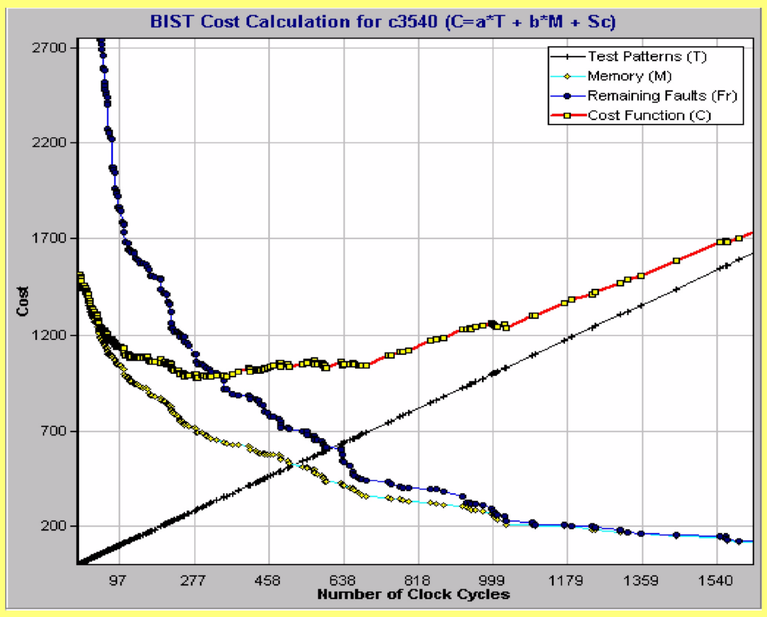
- A Hybrid BIST architecture that supports the combination of pseudorandom and deterministic test patterns in cost effective way.
- The architecture can be implemented only in software and is therefore flexible and well suitable for SoC designs.
- An approach to find the optimal balance between pseudorandom and deterministic test sets with minimum cost of time and memory, without losing test quality.
- Our approach can lead to significant decreases in overall test cost.

SoC Testing

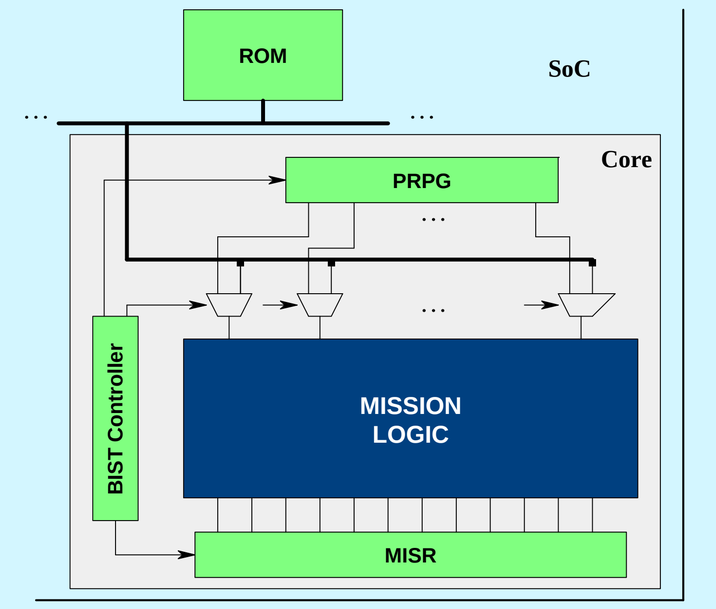


Total Cost Calculation

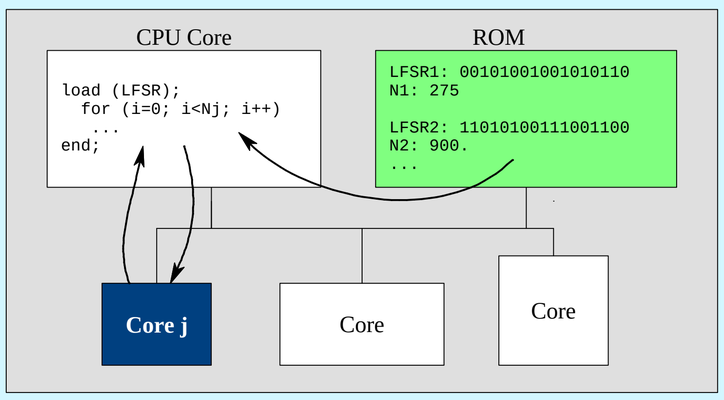




Hybrid BIST Architecture



Hardware Based Hybrid BIST Architecture



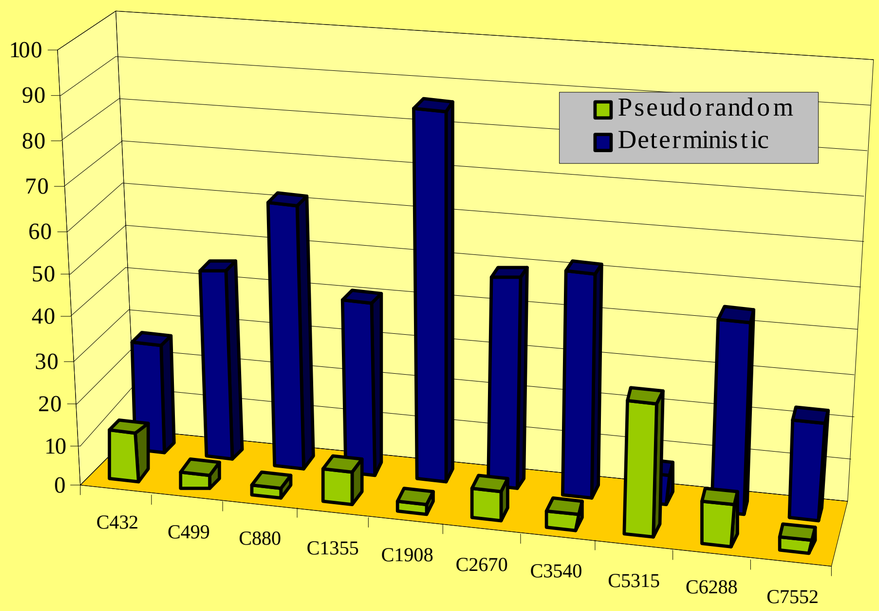
LFSR Emulation

Cost Calculation Algorithms

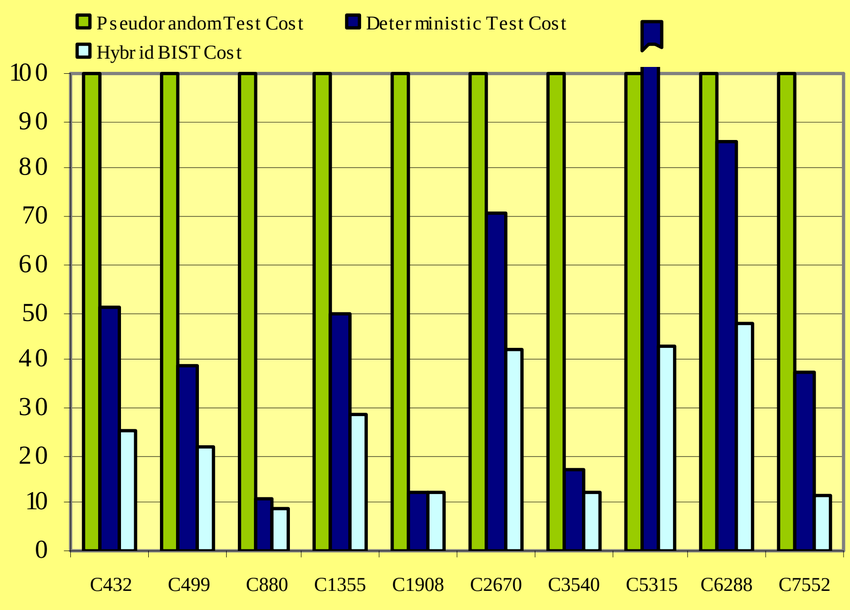
- Cost and efficiency of pseudorandom test can be calculated based on simulation results.
- Deterministic test set can be calculated by:
  - Using ATPG in the loop
  - Iteratively transforming fault tables.
- Optimal combination between pseudorandom and deterministic test vectors is found by using a Tabu search heuristic, which reduces the number of calculations significantly (in average 10 times) without losing in cost calculation accuracy (not less than 97,2%).

Experimental Results

- Hybrid BIST approach gives considerable reduction of cost compare to the pure pseudo-random or deterministic test.
- Typically less than half of the deterministic vectors and only a small fraction of pseudo-random vectors are needed.
- Fault coverage is not sacrified.



Percentage of test patterns in the optimized test sets compared to the original test sets



Cost comparison of different methods.
Cost of pseudorandom test is taken as 100%