Master Thesis –
Comparator Design for High-Speed ADCs

Background
Are you up for the challenge to develop next generation integrated circuits for our continued leadership in mobile communications? In radio base stations, high-speed analog-to-digital converters (ADCs) are required to handle wide band signals. A critical sub-circuit in ADCs is the comparator which performs the basic function of comparing two voltages. A challenge for comparator design is to obtain a very short decision time while keeping other key parameters such as power consumption, hysteresis, offset, and noise sufficiently low. In this thesis work you will study the latest state-of-the-art comparator architectures, implement some of them in schematics and compare them by simulations with aid of optimization tools.

Thesis Description
The following steps are envisioned as part of the thesis work:

- Literature survey to gain familiarity with high-speed comparators.
- Transistor schematic implementation of a few selected architectures from the literature studies.
- Verify basic operation of the selected architectures by simulations. Initial device sizing to make the different comparators functional.
- Optimize the selected architectures with help of optimization tools. Compare the results of the different architectures.

The thesis will be concluded with a result presentation for the Ericsson team.

Qualifications
- This project aims at students in electrical engineering, computer engineering or similar with interest in full custom integrated circuit design.
- Analog/digital circuit design basics (relevant coursework).
- Experience in transistor schematic design (Virtuoso IC) and circuit verification (Spectre simulator).
- Custom layout design experience (preferred but not mandatory).

Extent
1 student, 30hp

Location
Ericsson AB Mjärdevi, Linköping

Preferred Starting Date
Spring 2022

Keywords
Full custom, ASIC, CMOS, Data Converters, DAC, ADC

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