Master Thesis – Memory Hierarchy Modeling and Visualization of Execution Flows

Background
Mobile networks are used all over the world and are the cornerstone for the networked society, where everything will be connected. To support the vast amount and diversity of data expected in future networks, Ericsson develops products to drive and support the networked society. The subject for this Master Thesis is defined to investigate and develop algorithms, architecture, tools etc. to support huge increase of speech, data, and massive IoT for Radio Access Networks.

Thesis Description
Memory management is a large part of the cycles spent both for cloud and embedded applications especially for a highly dynamic control plane application. A model is needed to project application impact by different cache hierarchy, sizes, latencies, and memory allocators on different hardware.

The thesis will be concluded with a result presentation for the Ericsson team.

Qualifications
This project aims at students in electrical engineering, computer science, computer engineering or similar.

Extent
1-2 students, 30hp each

Location
Ericsson AB Mjärdevi, Linköping

Preferred Starting Date
Spring 2023

Keywords
SW development, Mobile Telecommunication, Optimization.

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