Master Thesis – Built-in Self-Test for Analog and RF Circuits

Background
Are you up for the challenge to develop next generation integrated circuits for our continued leadership in mobile communications? Integrated circuits require built-in self-test, BIST, blocks that supervise the circuits to detect potential problems. These blocks are used extensively and must be robust against PVT (process, voltage, and temperature) variations, and in addition also be easy to migrate between process nodes. The BIST blocks typically supervise input/output power, supply voltage, and supply currents. When a malfunction is detected, the right action must be taken to protect both the circuit and its surroundings. This thesis work includes, but is not limited to, the design and evaluation of two different BIST blocks; a power- and a current-detector.

Thesis Description
The following steps are envisioned as part of the thesis work:

- Literature survey to find current solutions and the state-of-the-art solutions
- Choose a suitable topology for transistor implementation (schematic) and critical parts in layout
- The selected solutions will be characterized, and strengths and weaknesses assessed
- The thesis work will be concluded with a presentation for the Ericsson team

Qualifications
- This project aims at students in electrical engineering, computer engineering or similar with interest in full custom integrated circuit design.
- Analog/digital circuit design basics (relevant coursework).
- Experience in transistor schematic design (Virtuoso IC) and circuit verification (Spectre simulator).
- Custom layout design experience (preferred but not mandatory).

Extent
1-2 students, 30hp

Location
Ericsson AB Mjärdevi, Linköping

Preferred Starting Date
Spring 2023

Keywords:
Full custom, ASIC, BIST, CMOS, Data Converters, DAC, ADC

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