Complexity Challenges towards 4th Generation Communication Solutions

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Infineon Technologies AG

Never stop thinking

Outline

- Introduction: Embedded Computing for Wireless Handhelds
- Embedded System Architecture Challenges
- Component-based Approach
- Summary and Conclusions

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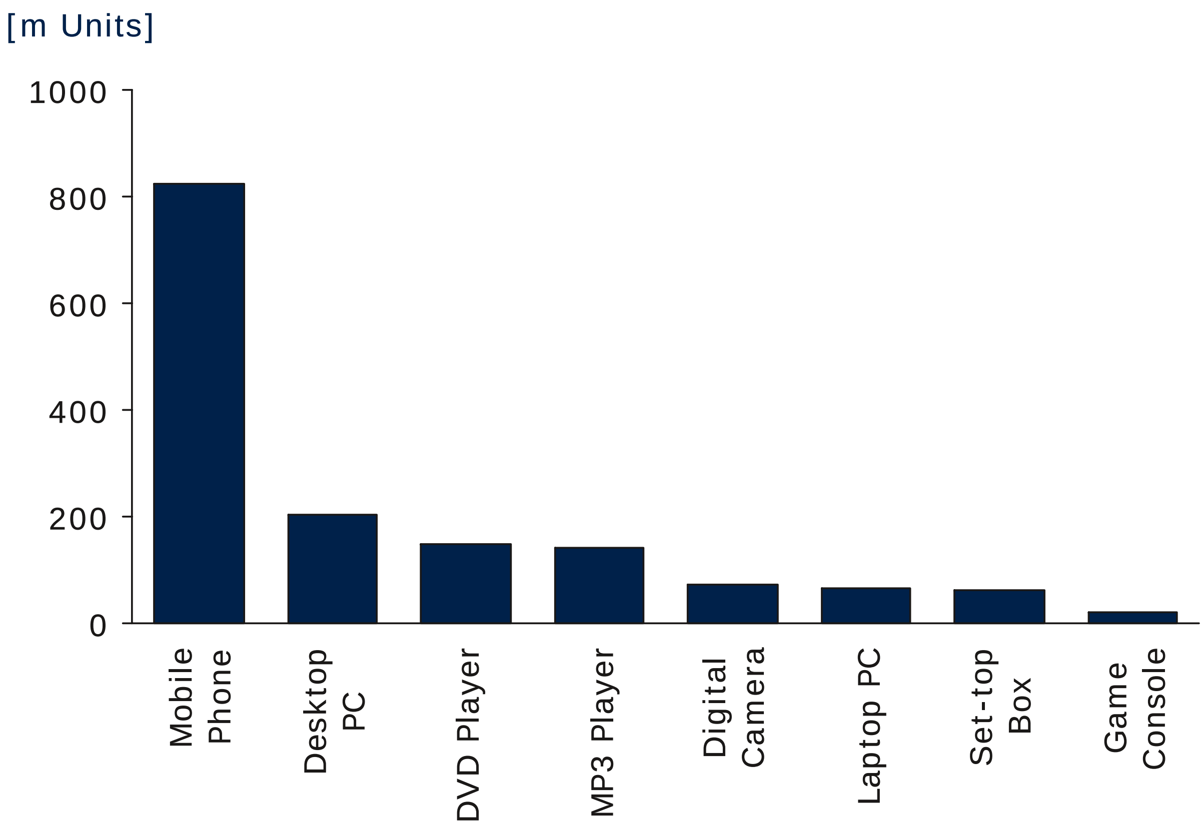
Moving on to Multimedia Communication

Electronic Market
The Biggest Application is Mobile Telephony

Sold Pieces of selected Applications per Year (2005)

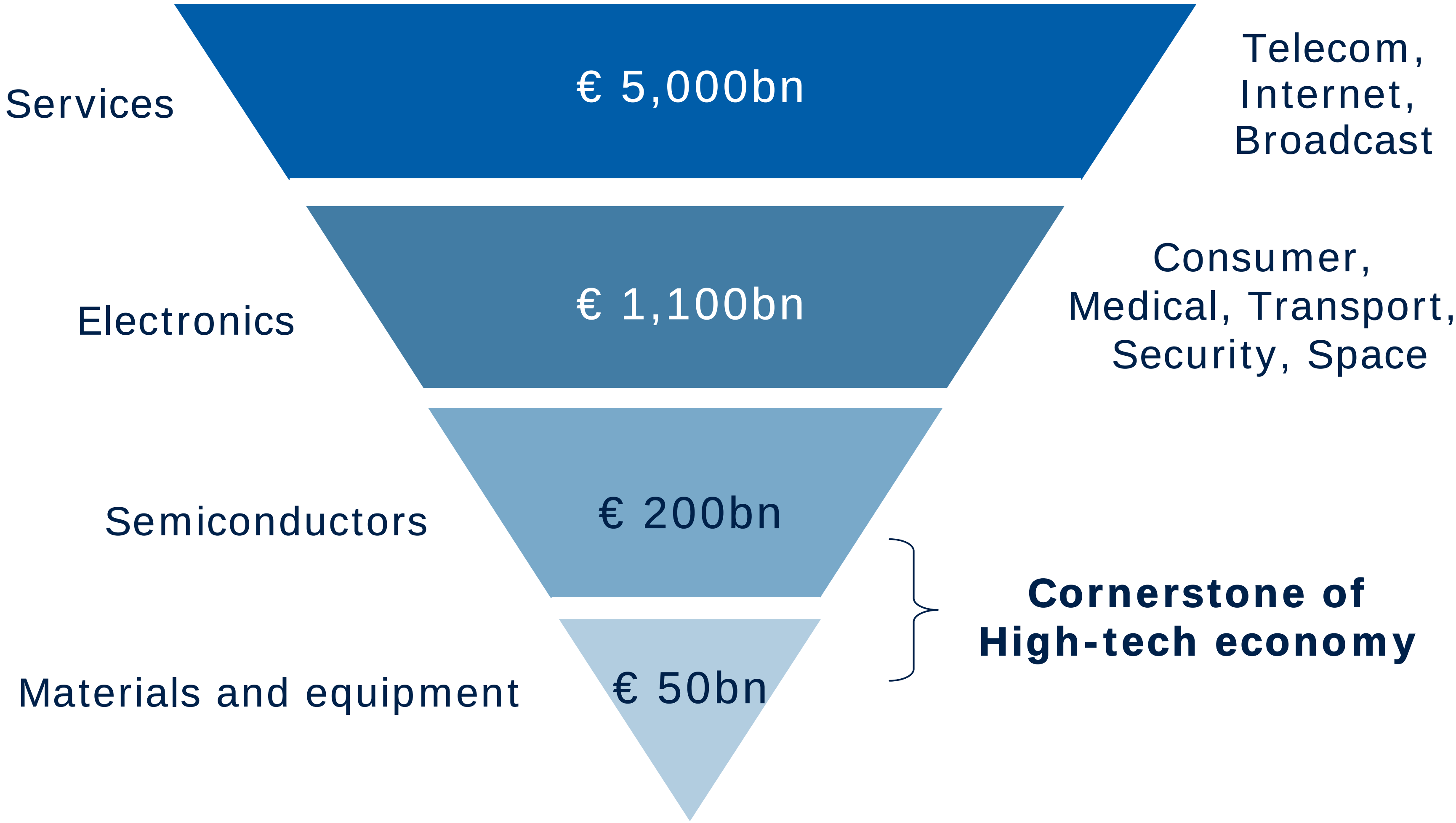


Comment

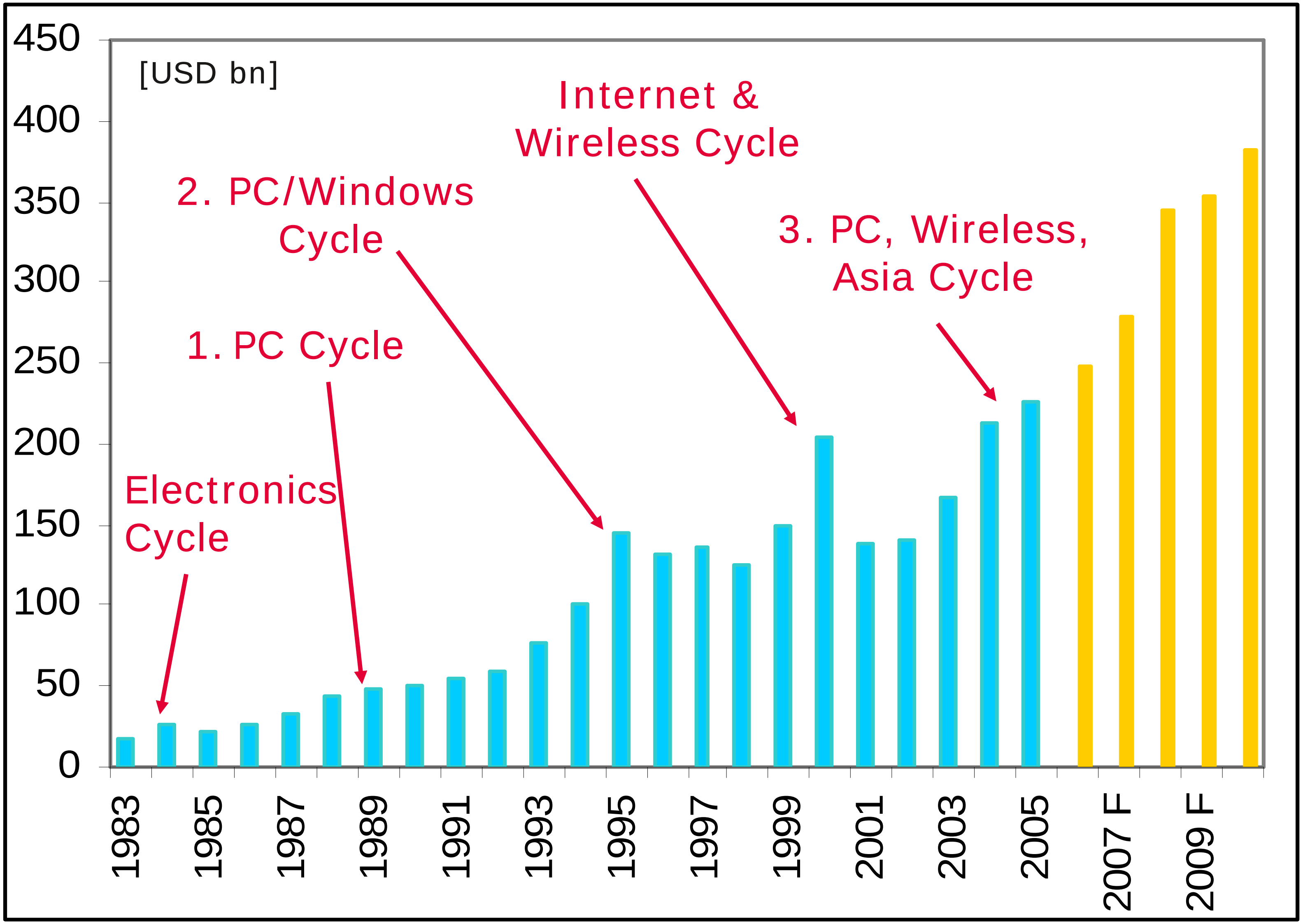
- Mobile phone segment is by far the largest segment for end user devices and thus a key market for embedded processing devices
- Mobility and device convergence drive requirements for low power, computing performance and user experience

Source: CIBS World Markets Digital Media Bible March 2006

Industrial Landscape

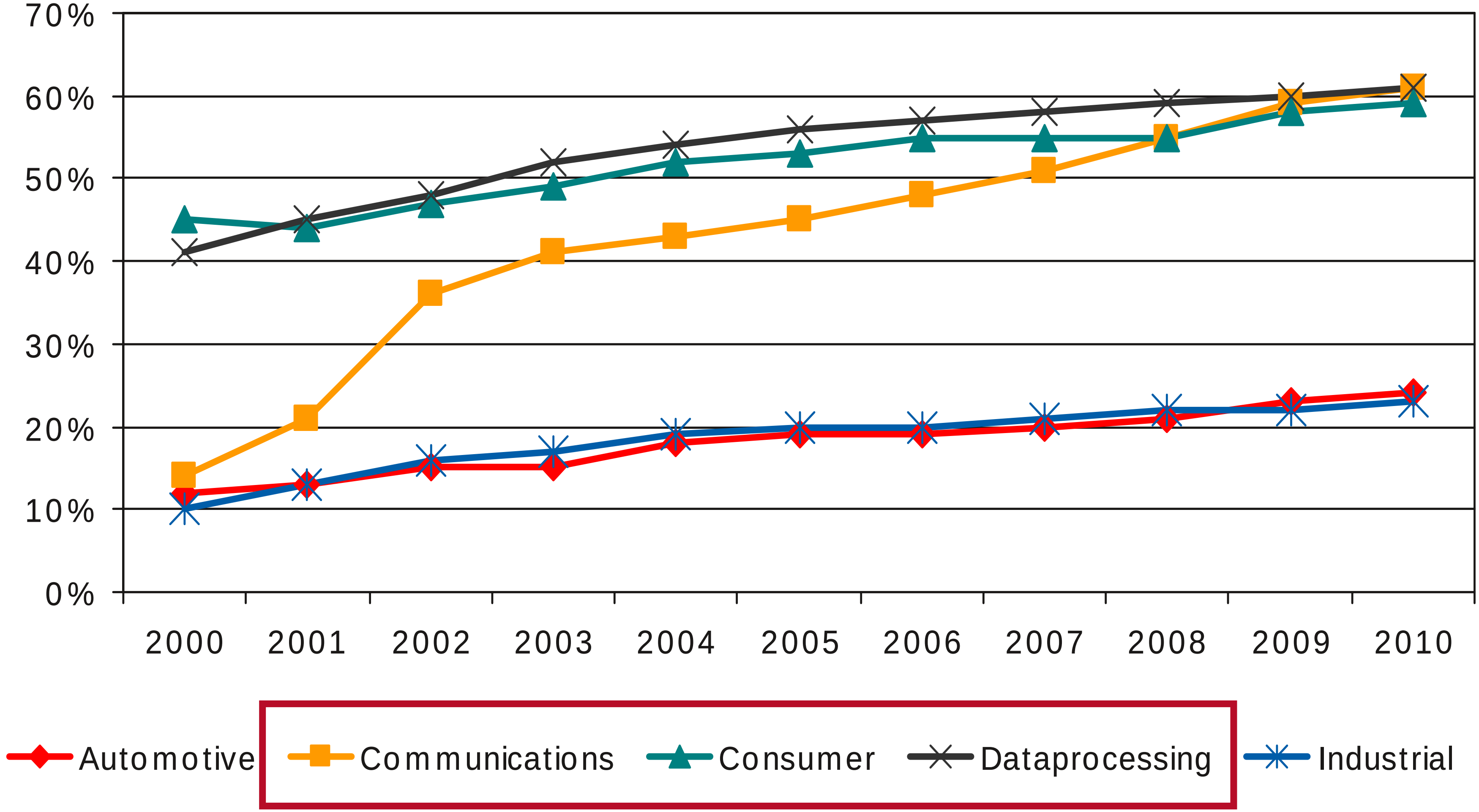


Semiconductor Industry Size



Source: WSTS, McClean Report 2006, UBS Primer

Evolution of Asia's Share in Electronic Equipment Manufacturing per Industry Segment



Source: Gartner

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The Evolution from GSM towards UMTS
UMTS - The Enabler for Real Wireless Multimedia

"Historical" view

	GSM	GPRS / EDGE	UMTS
	2nd Generation	2.5nd Generation	3rd Generation
Data Rate	■ 9.6 kbps	■ 115 kbps ■ 384 kbps	■ 384 kbps ■ 2 Mbps
Applications	■ Voice ■ SMS	■ E-Mail ■ Data-Services	■ Multimedia Services ■ Interactive Games
Products	■ Phones	■ Smart Phones ■ PDAs	■ Mobile Multimedia Terminals

Few Simple Criteria Drive the Development of Mobile Handset Architectures

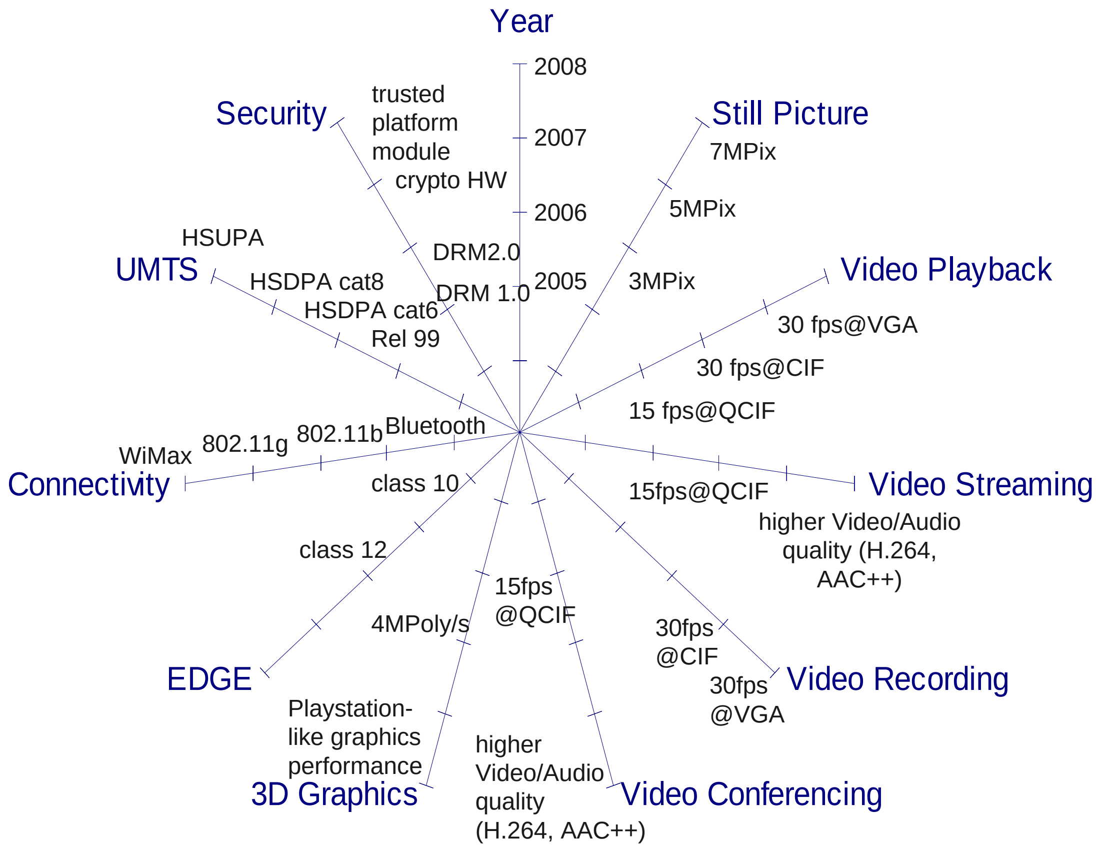
Quality
- Power consumption
- User experience

Features
- Multimedia
- Display resolution
- Audio
- Interfaces

Design
- Smaller form factor
- Fashion

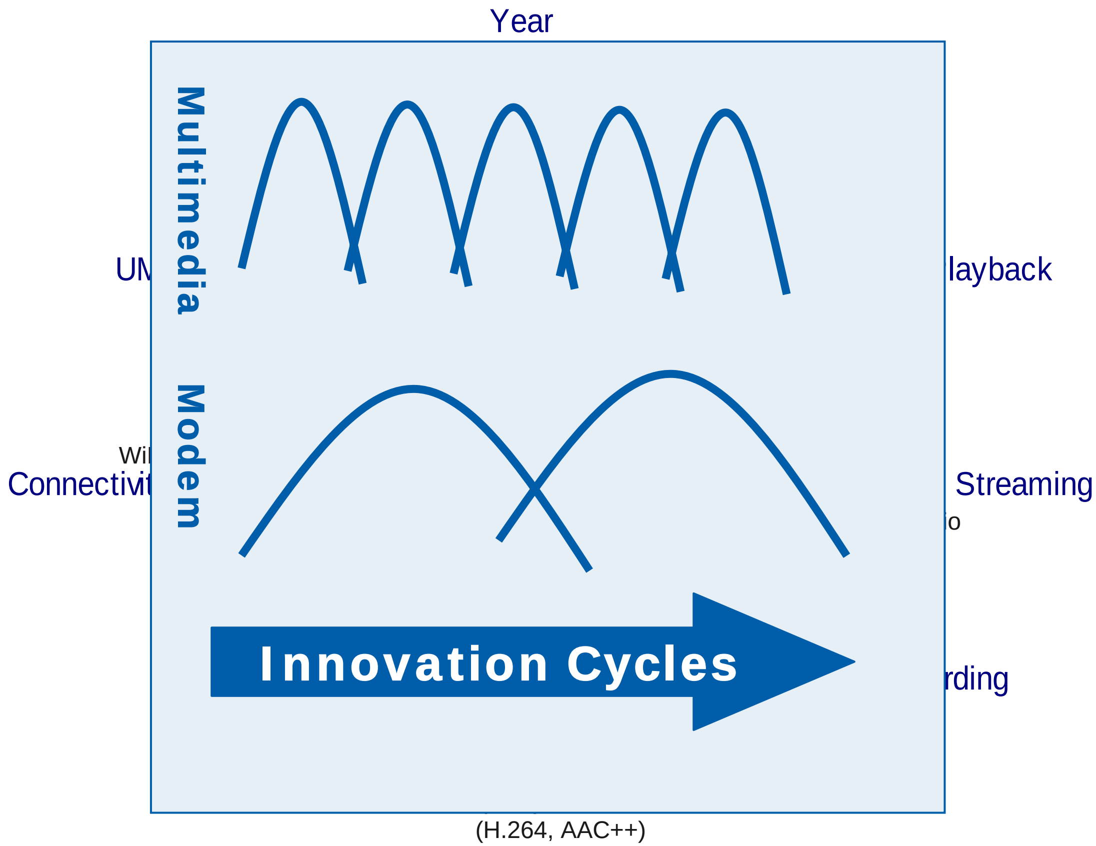
Scalability
- Recognizable look and feel
- Branding

Feature Requirements are Getting More Complex



Growing number and complexity of mobile phone features needs to be handled in a structured way

Feature Requirements are Getting More Complex



Growing number and complexity of mobile phone features needs to be handled in a structured way

Mobile Device is Becoming an „All-In-One Solution“

3D Graphics

Sensors

Security

Camera

Video conferencing

Audio

UWB

WiMAX

WLAN

Bluetooth

HSDPA

DVD

DSC

Digital TV

Camcorder

Gaming

Music/MP3

Mobile Device is Becoming an „All-In-One Solution“

3D G

(Hard) Real-time requirements
- Wireless radio access
- Audio and UI processing
- Power management

Camera

Constraint resources
- Battery (low-)powered
- Limited processing performance
- Limited memory
- Limited space

WiMAX

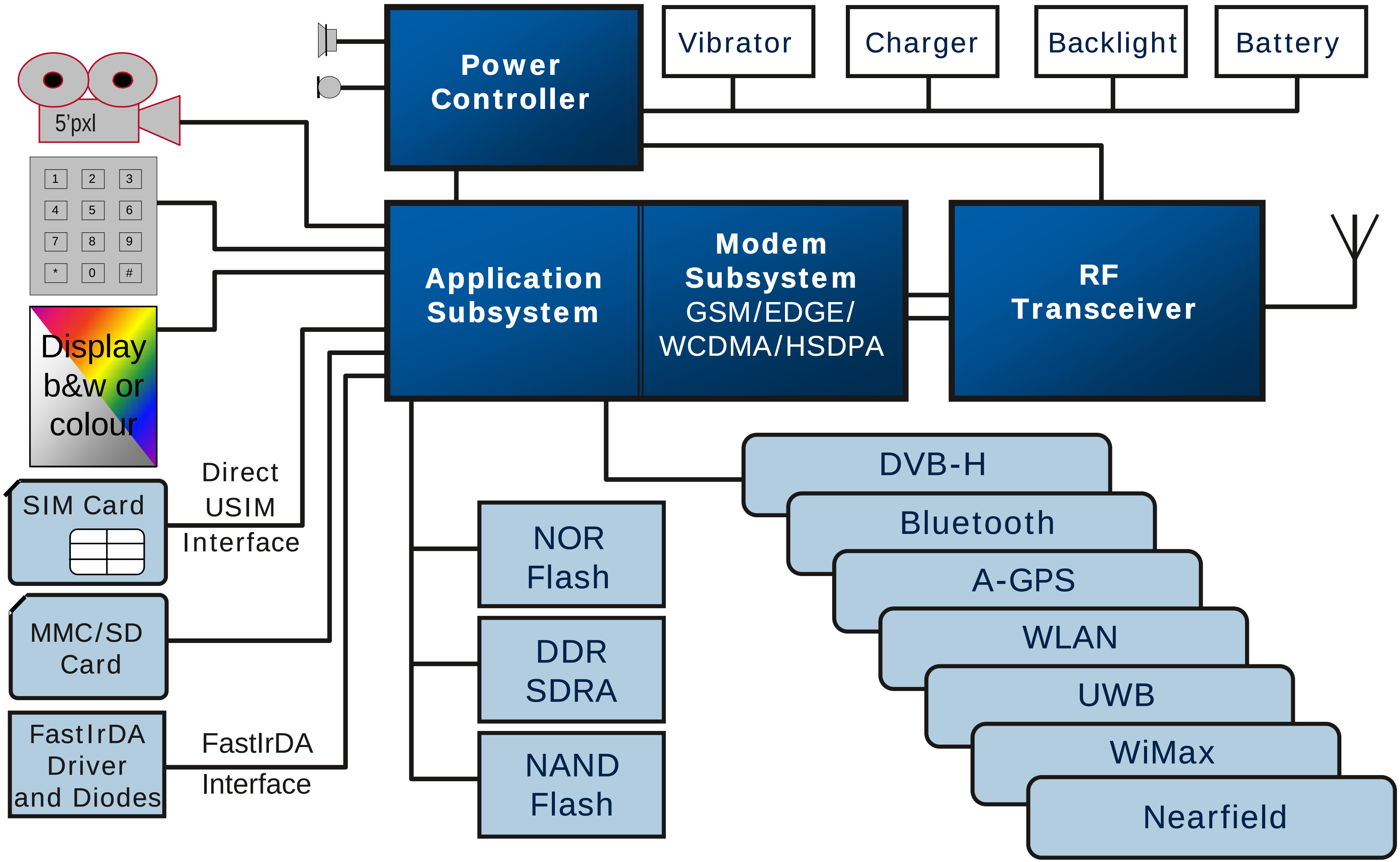
Camcorde
r

Integration of multiple subsystems

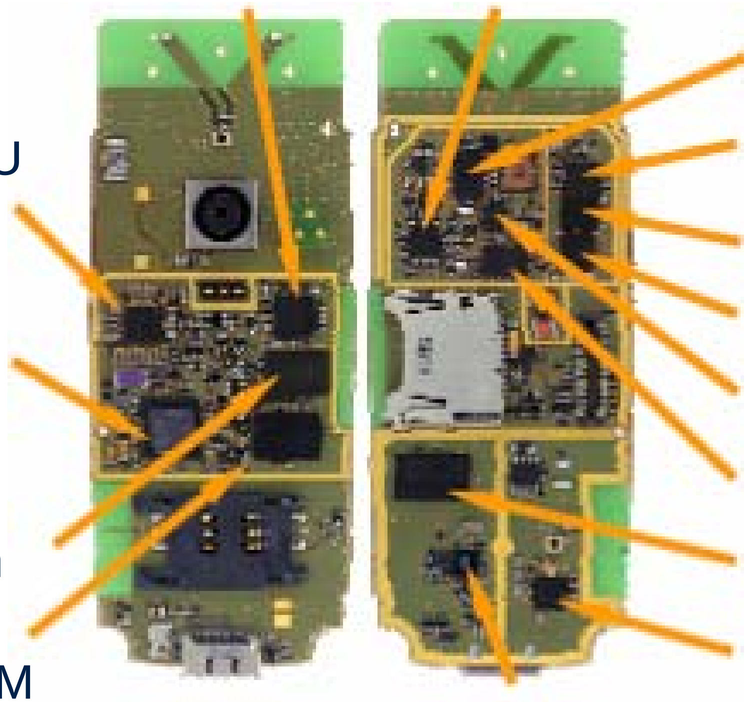
HSDPA

Music/MP3

Future Mobile Phone Content



Future Mobile Phone Content Limited by Board Space



3G Co-Processor

3G TRX

PMU

GSM BB Processor

SIM-Card

NOR-Flash

SD-RAM

FM-Radio

UMTS PA/Band 2

GSM/EDGE TRX

FEM

GSM/EDGE PA

UMTS PA/Band 1

UMTS PA/Band 5

NAND-Flash

Bluetooth Modem

WLAN

UWB

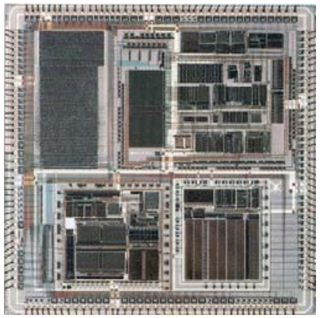
GPS

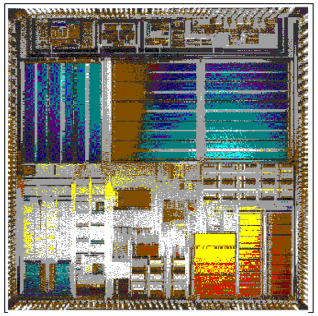
DVB

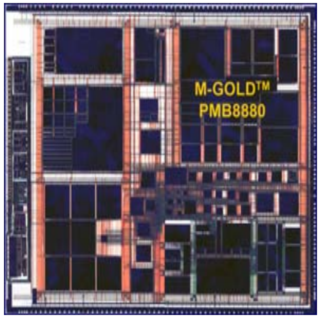
WiMax

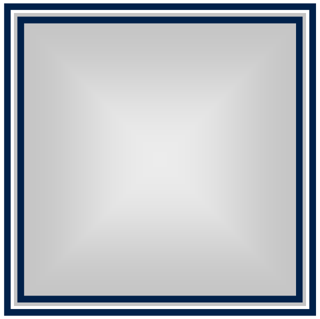
Moore's Law: Ever Increasing VLSI Power

GSM Modem	GSM, GPRS, EDGE Modem + Application	GSM+UMTS Modem	GSM, UMTS HSDPA, Bluetooth, WLAN, GPS, DVB-H
1µ CMOS 50k Tr.	0.25µ CMOS 11M Tr.	0.18µ CMOS 40M Tr.	nm CMOS 1B Tr.



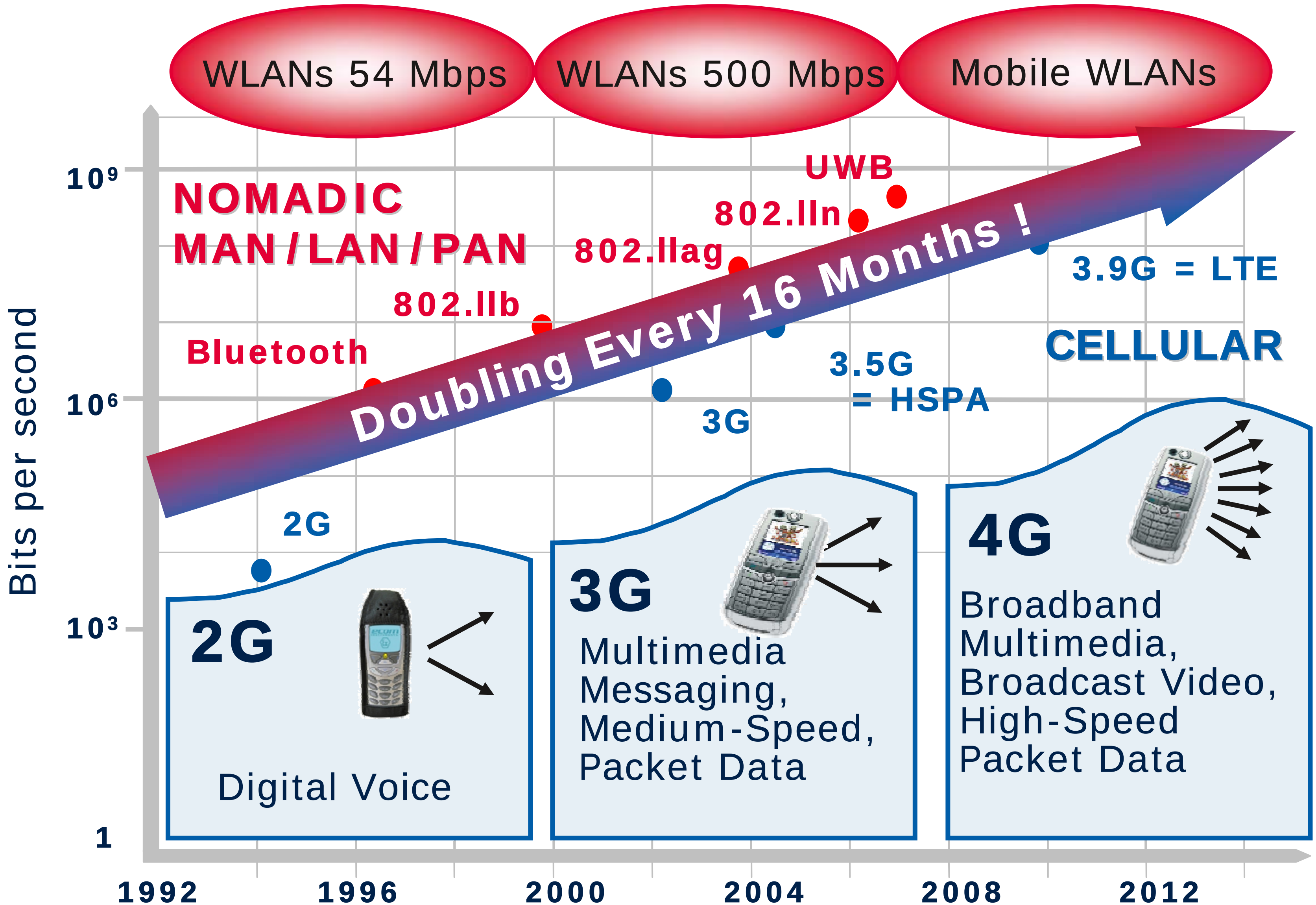




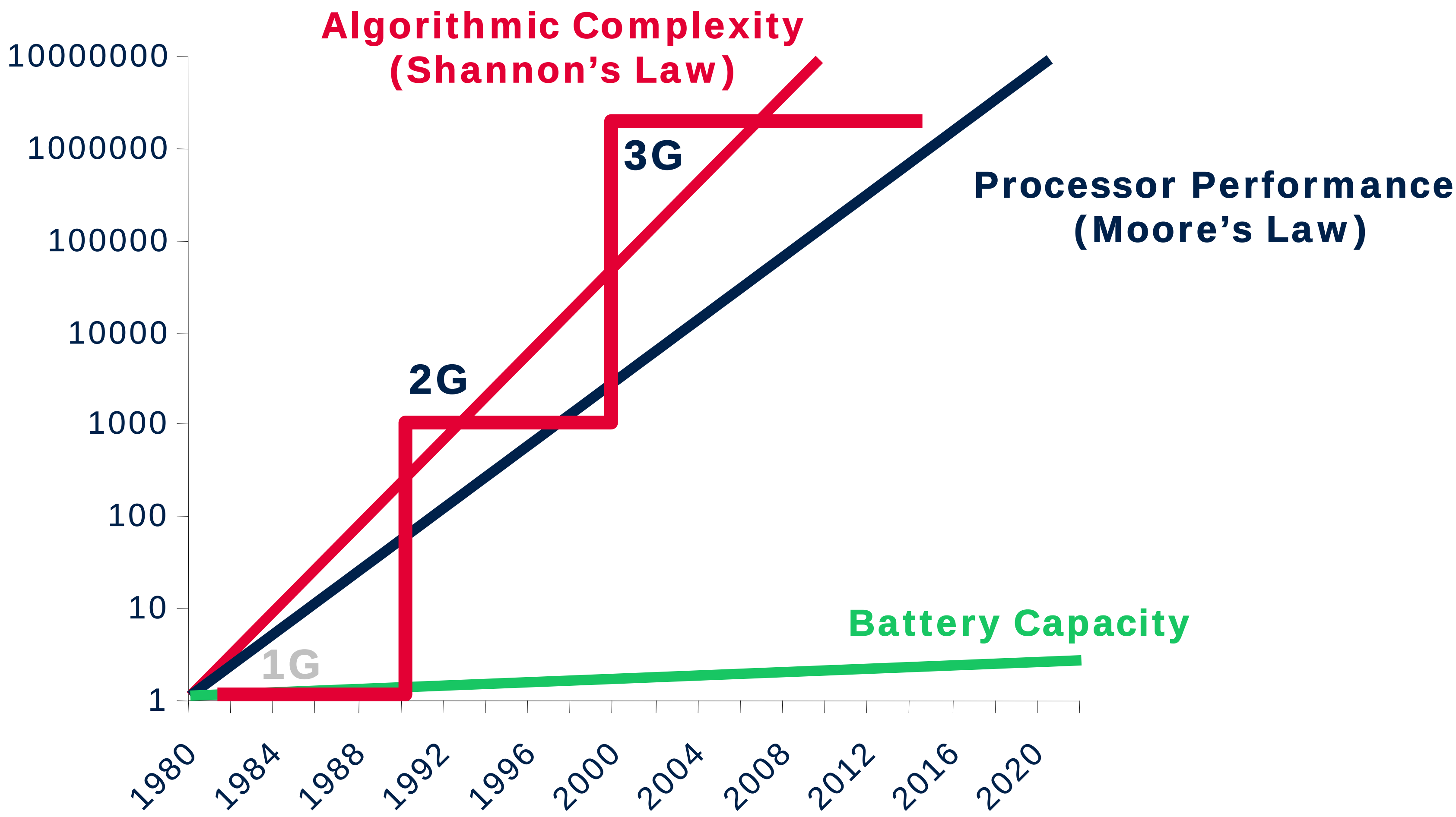


0.1 — 1 — 10 GIPS

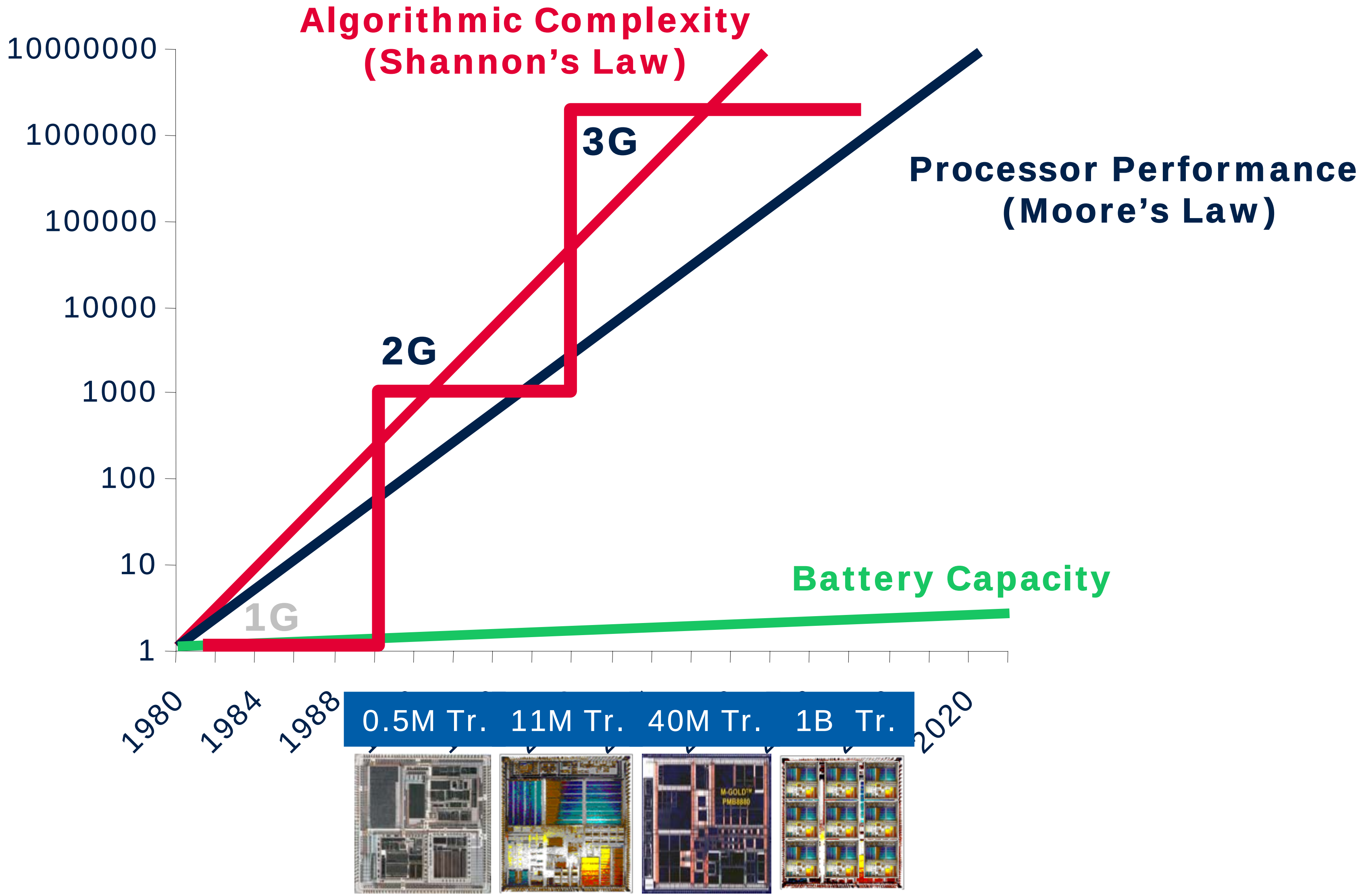
Mobile Pentium (~10W)


WLANs 54 Mbps
WLANs 500 Mbps
Mobile WLANs
10^9
10^6
10^3
1
Bits per second
NOMADIC
MAN / LAN / PAN
UWB
802.11n
802.11ag
802.11b
Bluetooth
Doubling Every 16 Months !
3.9G = LTE
CELLULAR
3.5G
= HSPA
3G
2G
2G
Digital Voice
3G
Multimedia
Messaging,
Medium-Speed,
Packet Data
4G
Broadband
Multimedia,
Broadcast Video,
High-Speed
Packet Data
1992
1996
2000
2004
2008
2012

The Algorithmic Driving Force



The Algorithmic Driving Force



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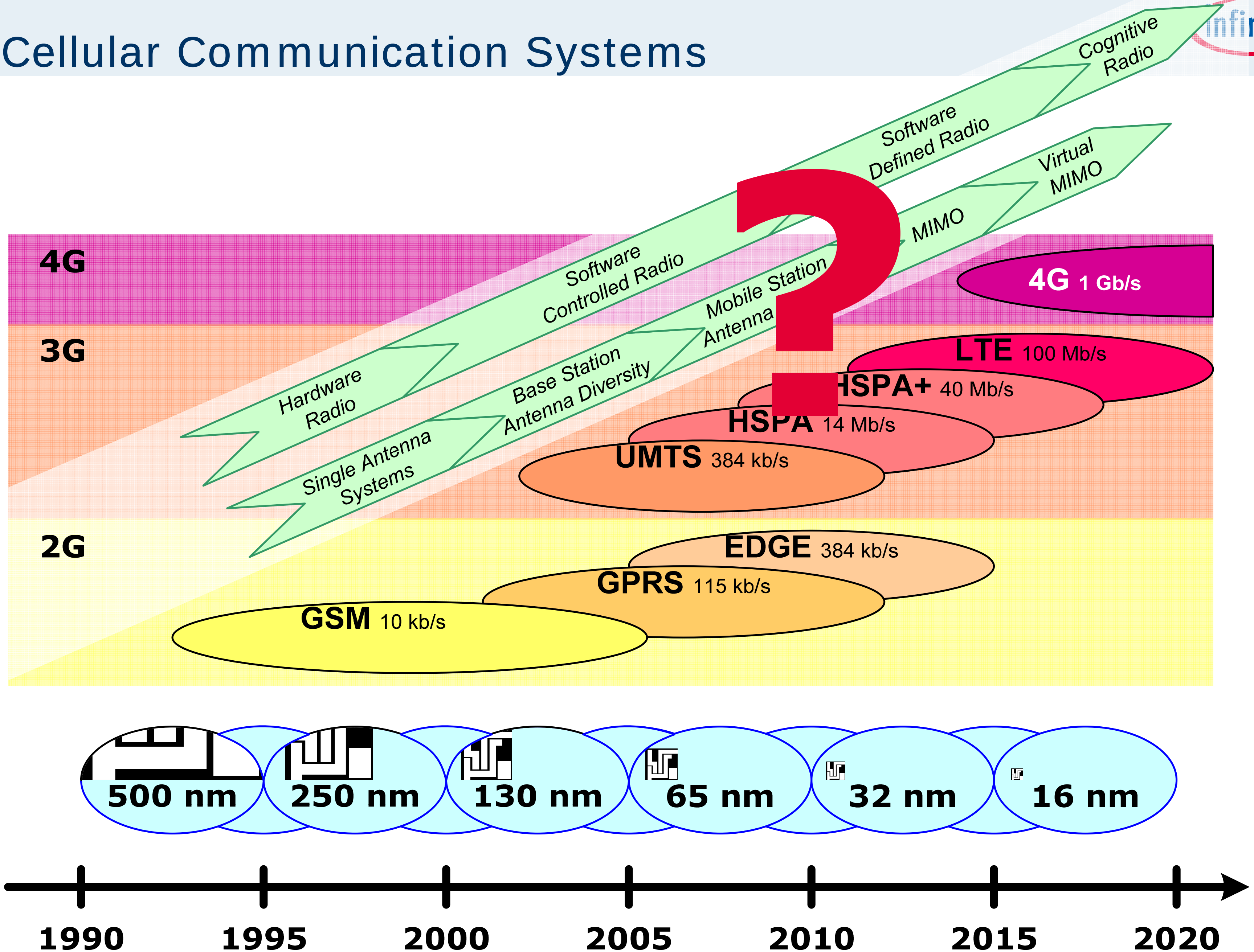
Cellular Communication Systems

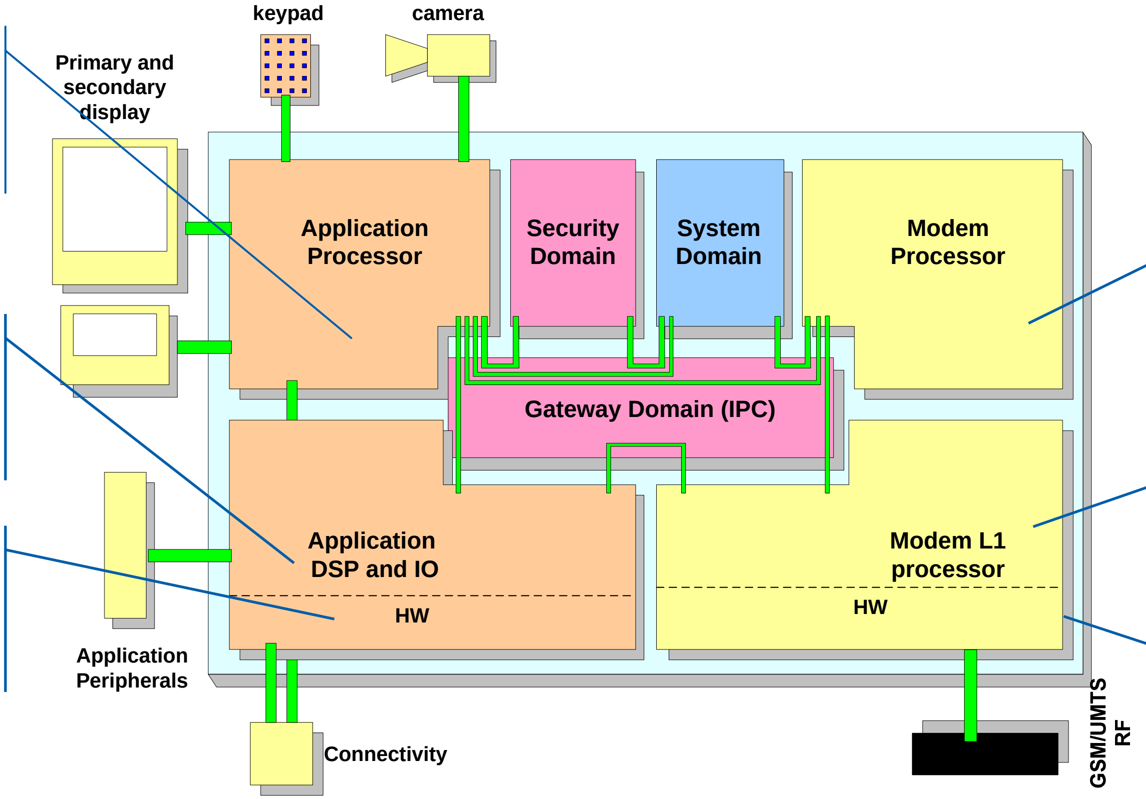


Processing Platform System/SW View

Application processing (“MIPS”)

Slot or Frame-based processing (~kHz rate)

Symbol and slot based processing kHz...MHz rate



Higher layer procedures (ms rate)

Slot or Frame-based processing (~kHz rate)

Symbol and slot based processing KHz...MHz rate

- Divide and conquer approach:
  - Cluster subsystems with similar computing and real-time properties
- Challenge for the conqueror: Integration

General Modeling Approach

SW development Architecture decisions

Early performance estimates

System validation & optimization

Virtual Prototype

High Level Model

Live Measurements

Use case data
CPU load
cache hit rates
power data

Performance & power targets

Use case data
CPU load
cache hit rates
power data

Project life

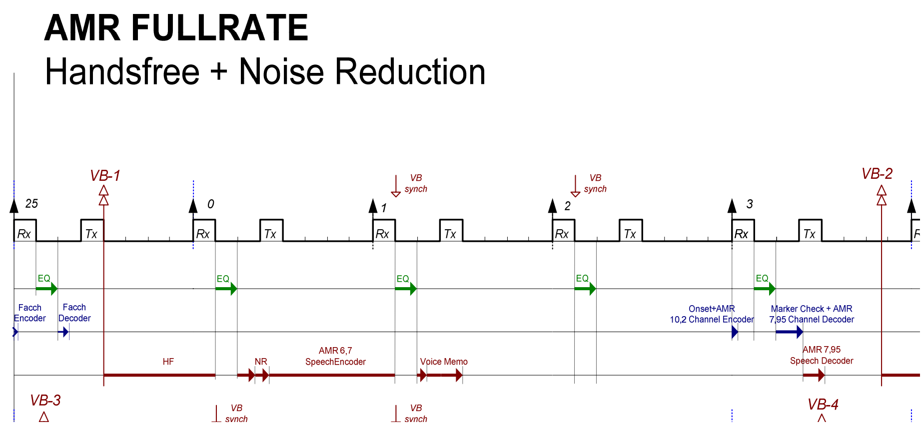
Begin to end

Begin to running system

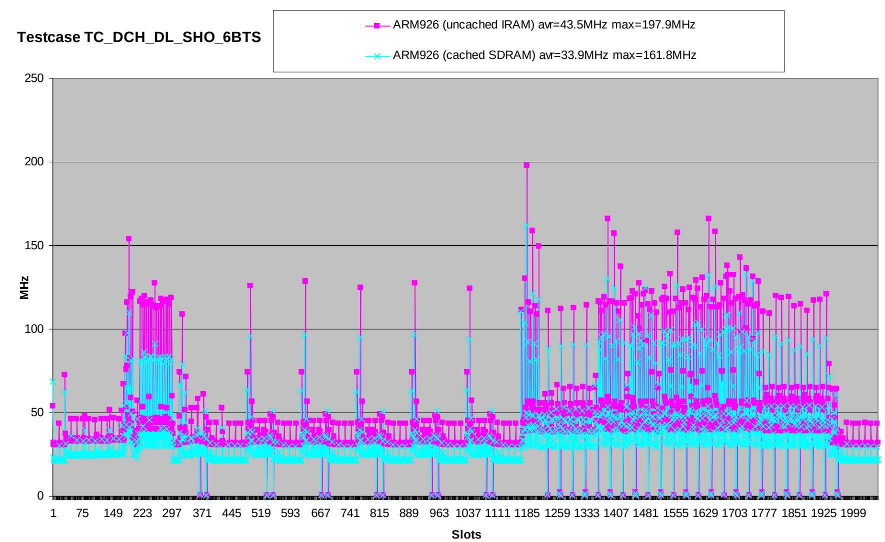
Running system to end

Complex Behavior of New Mobile Standards Require Prototype Models

- 2.75G L1 Firmware
  - Scheduling according to timing analysis (clustering of periods, interrupt driven, non-pre-emptive)
  - Uses hardware accelerators
  - Communication scheme GSM slot based
  - Simple performance model
    - Overall processing power



- 3.5G L1 processing
  - Controls low level physical layer procedures
  - Several HW accelerators involved
  - RTOS based implementation
  - Model generated through tracing and virtual prototyping
    - Event statistics



Complex Behavior of New Mobile Standards Require Prototype Models

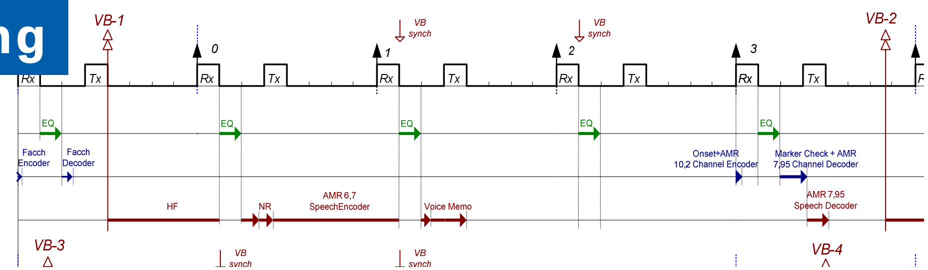
- 2.75G L1 Firmware
  - Scheduling according to timing analysis (clustering of periods, interrupt driven, non-pre-emptive)

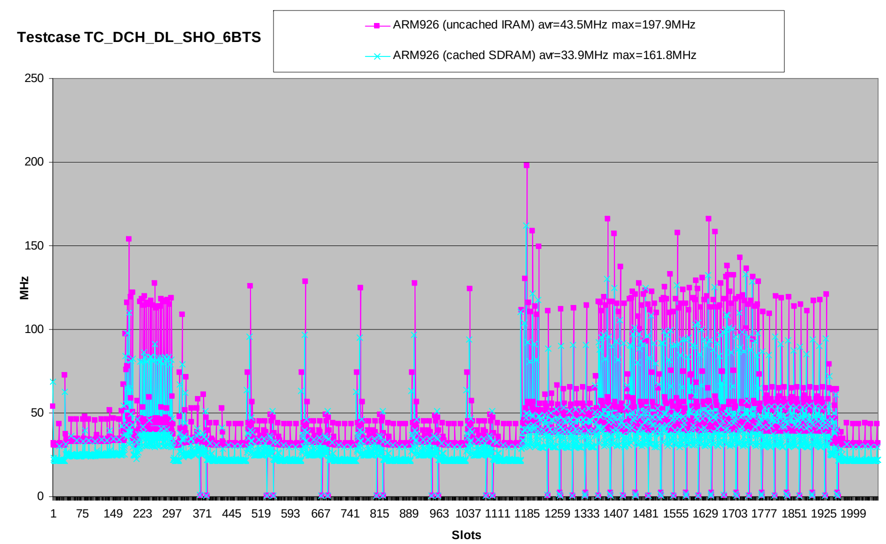
Deterministic real time scheduling

  based
  - Simple performance model
    - Overall processing power

AMR FULLRATE

Handsfree + Noise Reduction





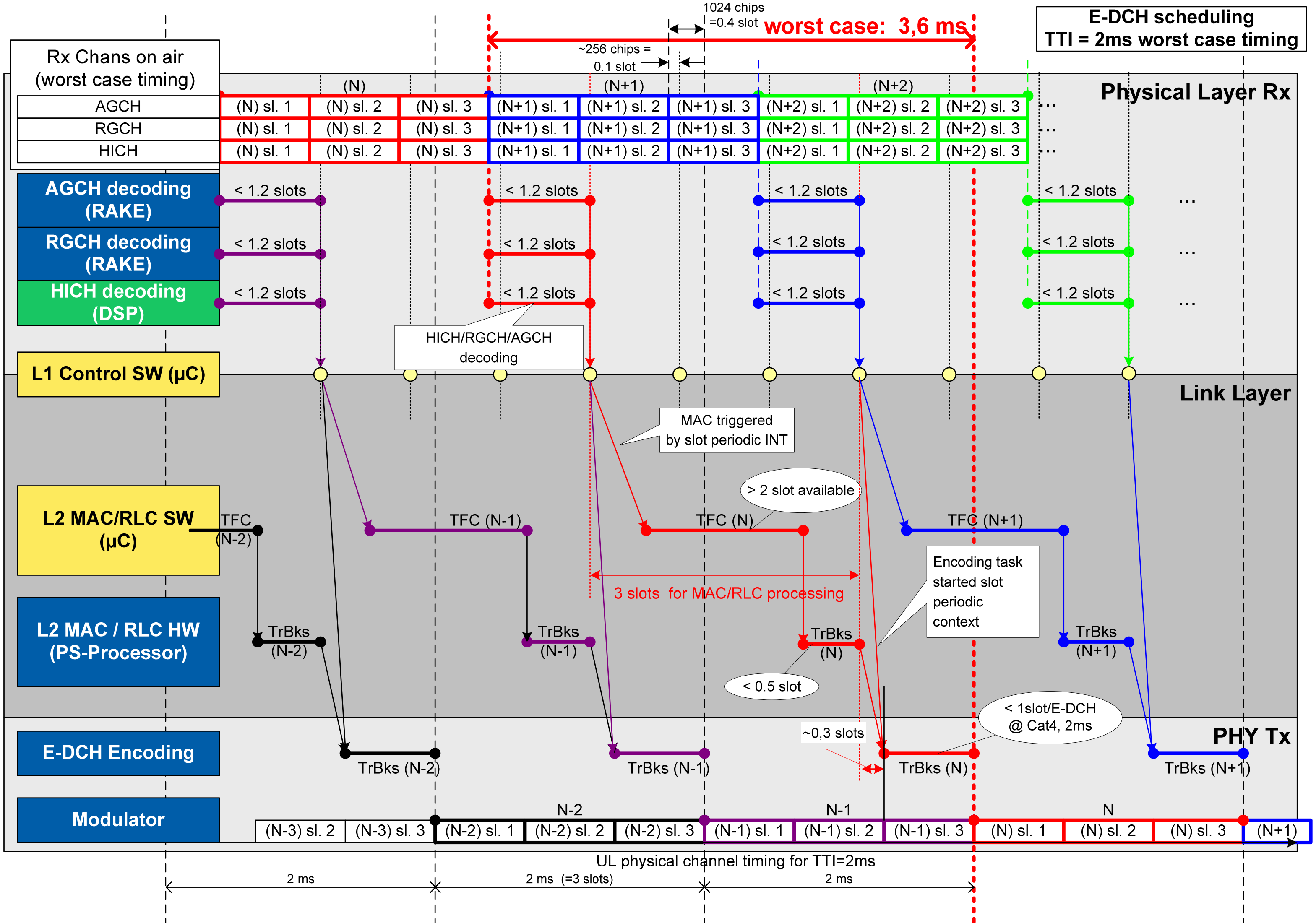
- 3.5G L1 processing
  - Controls low level physical layer procedures

Complex timing scenarios

  - RTOS based implementation
  - Model generated through tracing and virtual prototyping
    - Event statistics

HSUPA Timing Diagram (Simplified)

Loop: Air ➔ L1 ➔ L2 ➔ L1 ➔ Air



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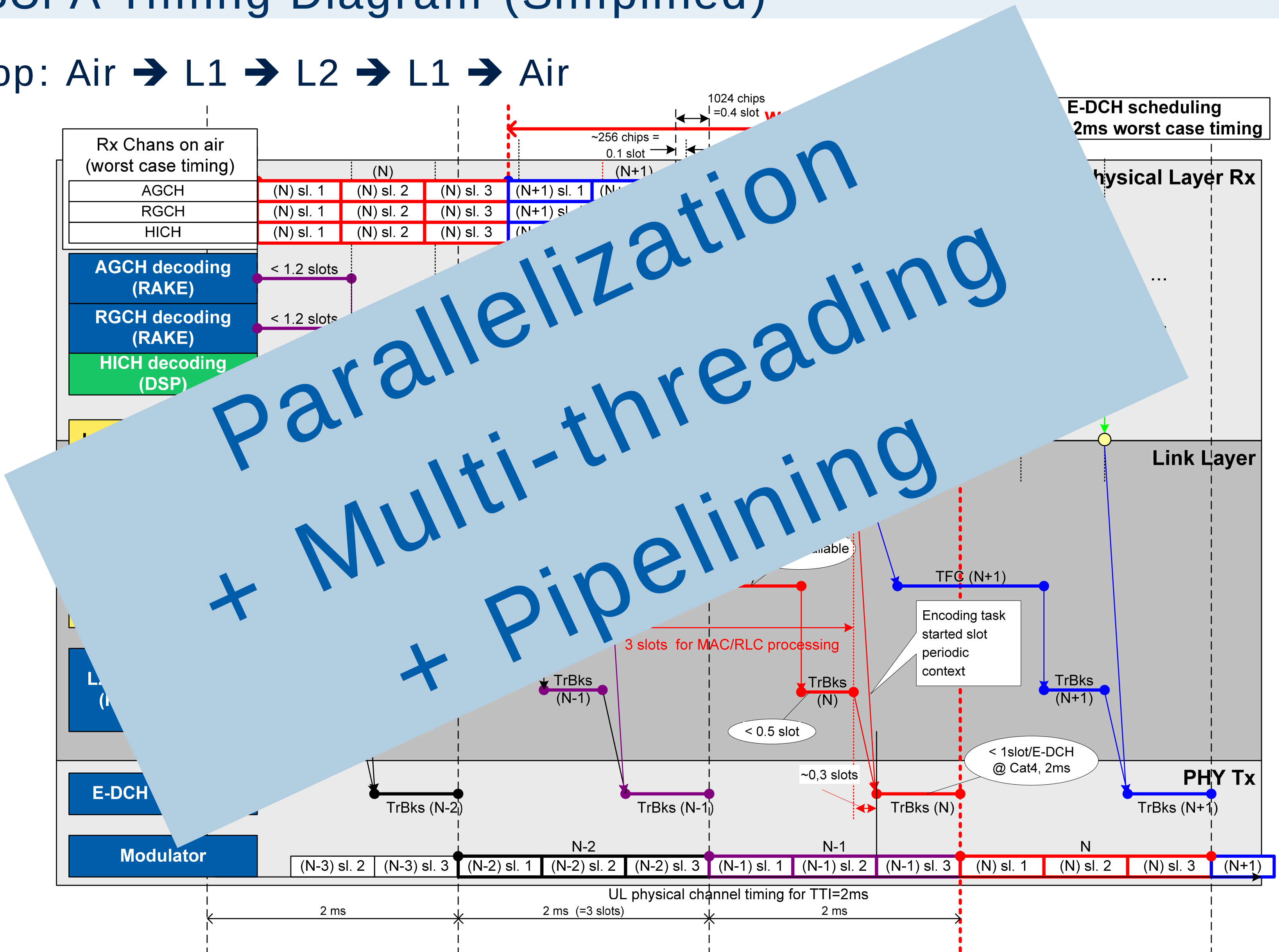
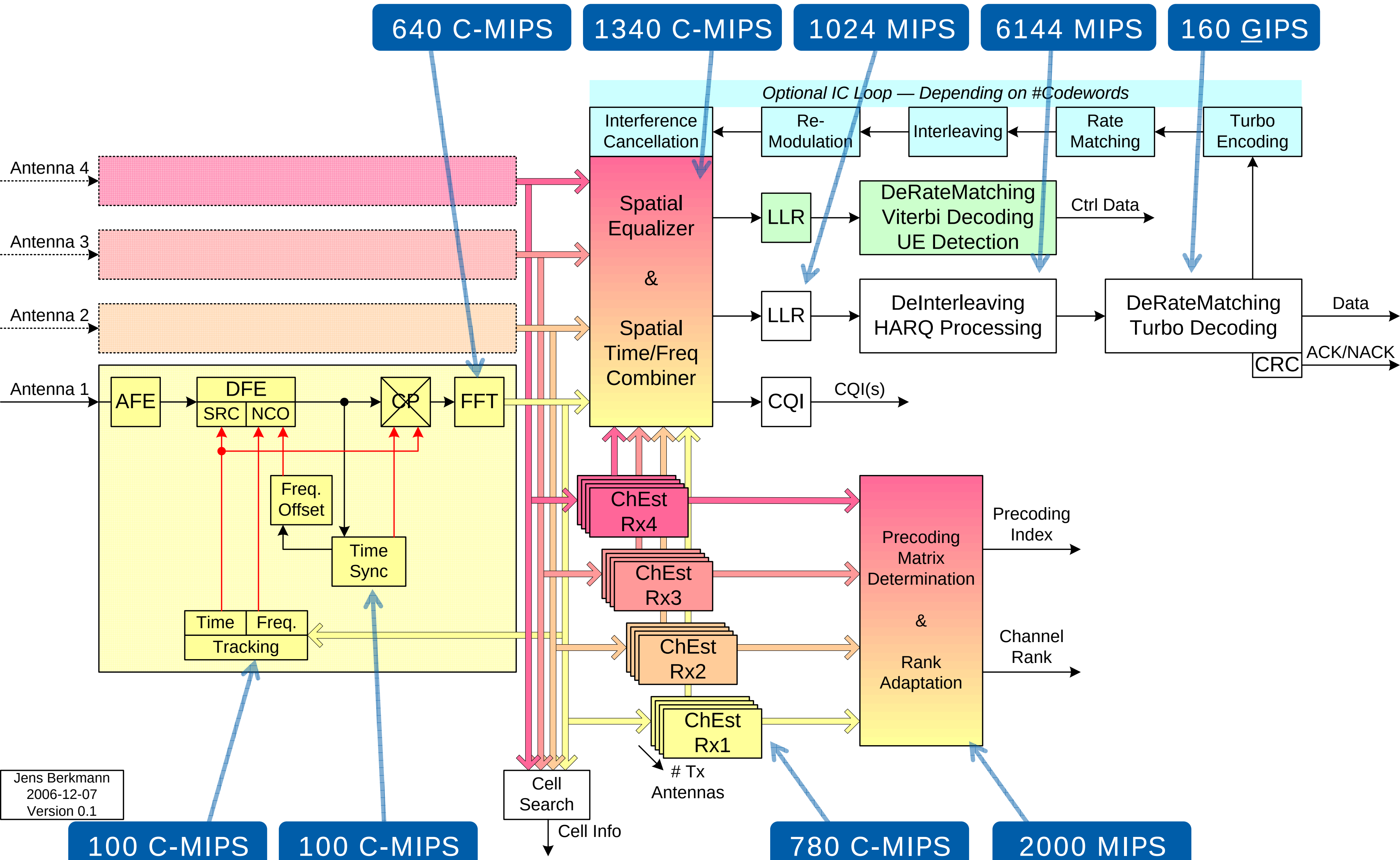
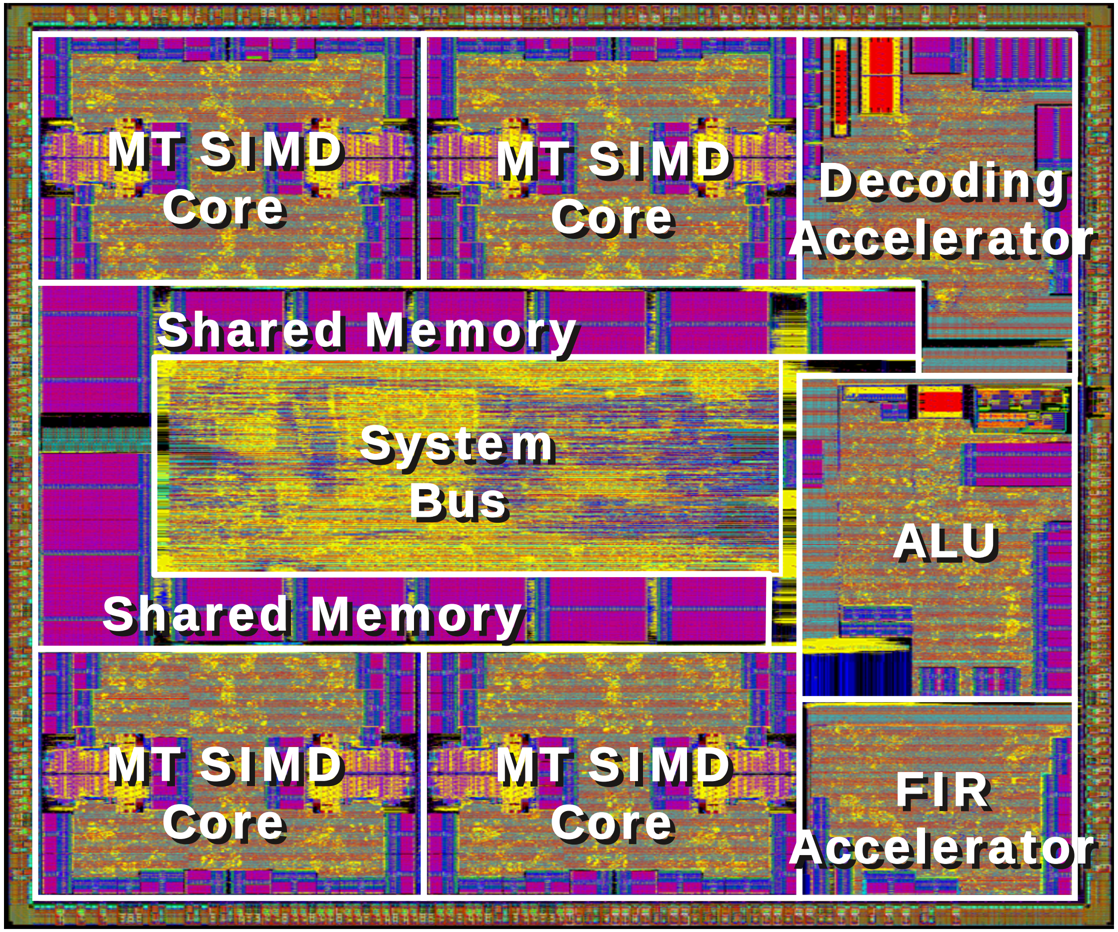
Loop: Air ➔ L1 ➔ L2 ➔ L1 ➔ Air



LTE
Physical Layer Complexity (4x4 Configuration)



Programmable Baseband Processor



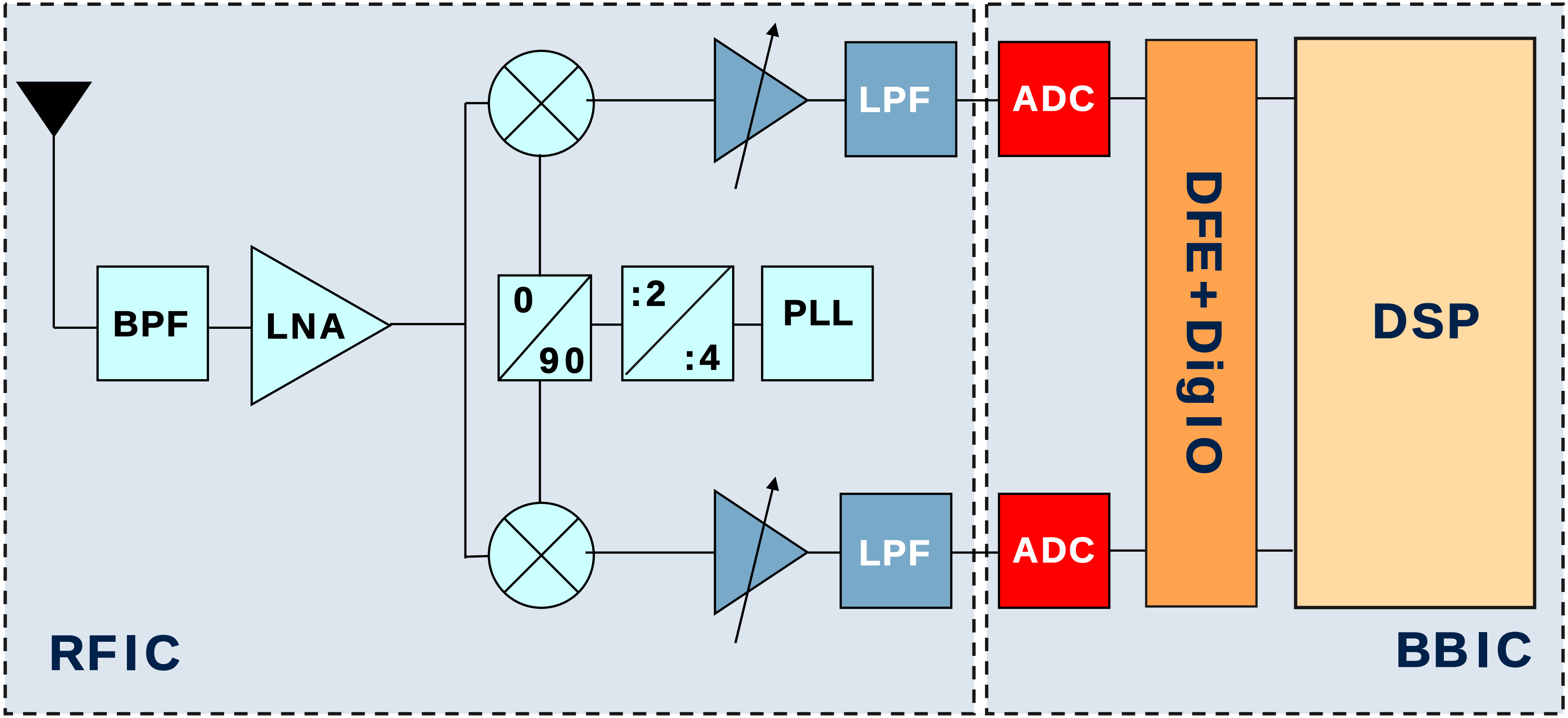
- 90nm CMOS
- Multi-Mode Capability
- Scalable by adding
  - MACs
  - ALUs
  - Memories
  - Accelerators
- Low Power Architecture

MT SIMD = multi tasking, single instruction, multiple data

RF - Challenges

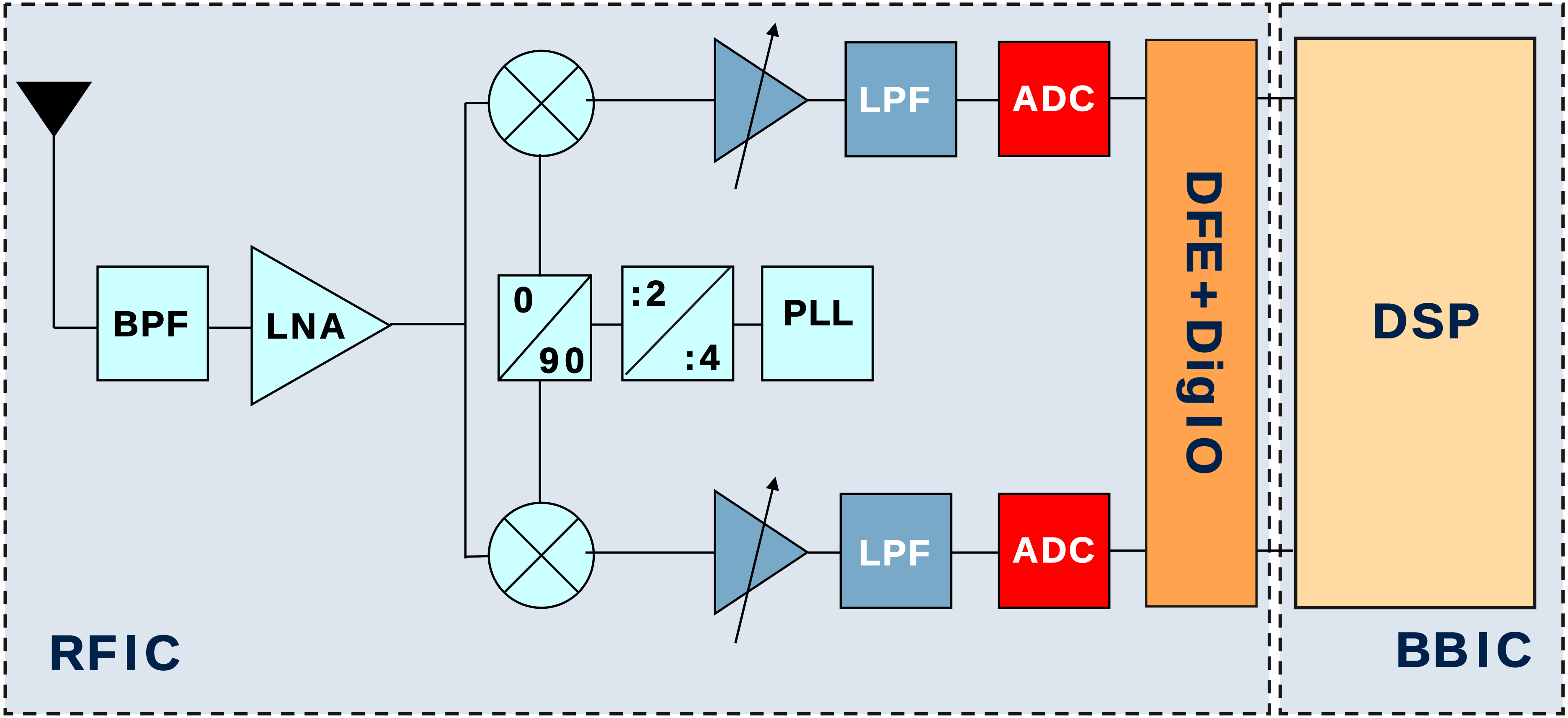
- Cover Frequency Band up to 77 GHz
  - Highly selective filters for many bands needed
  - ⇨ "Frontend Challenge"
- Flexible Reconfigurable High Performance Radio
  - Multiple Radios on One Chip
  - Multi-band RF engines (complex control scenarios)
  - MIMO Systems (demanding control loops)
  - ⇨ "Multi-Mode/Multi-Band Challenge"
- Electromagnetic Design on Chip
  - ⇨ “Power-Amplifier Challenge”
- RF SoC Design and Simulation Methodology
  - ⇨ “Complexity & Verification Challenge”

State-of-the-Art Analog DCR Architecture



- Analog channel selection
- Analog IQ interface
- Technology for the BB-IC needs to have an analog option

Extension of the DCR by an ADC, DFE and a Digital IQ Interface



- Channel selection moved to the digital domain
- Increased ADC requirements
- RF impairment correction in the digital domain

SMART RF Transceivers
Changed Digital/RF Split for Programmable RF Engines

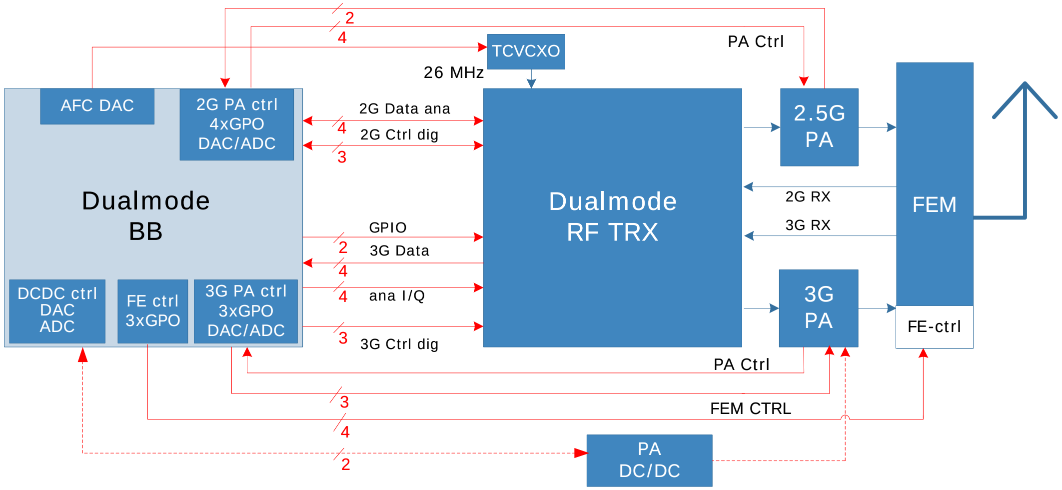
Approach

- Multimode and Multi-standard topics
  - RF front-end control complexity
  - High load on BB to close control loops
  - Link of RF and BB innovation
- Approach: Move some RF-related baseband processing functions into transceiver
- Results in autonomous RF engine design

Benefits

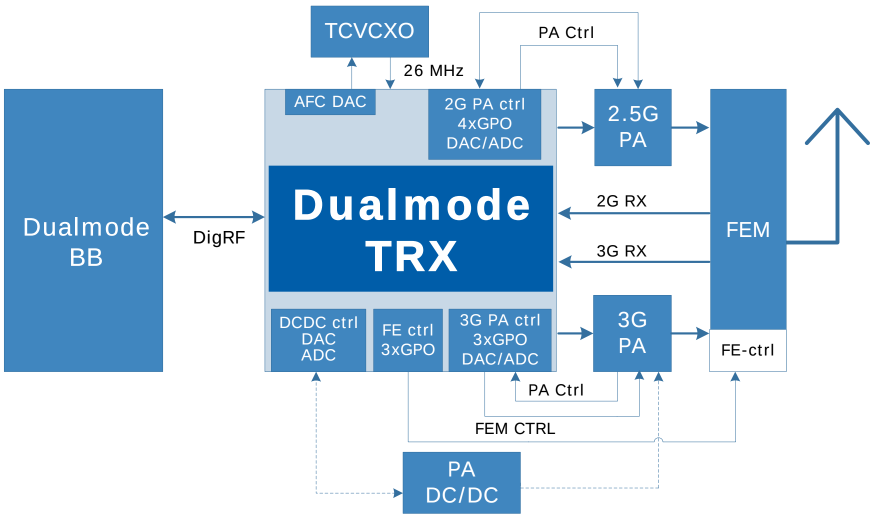
- Platform development in shorter time and reduced costs (SW development savings)
- Reduced production line calibration time and investment needed (ca. 20%)
- Improved System performance e.g: Faster IRAT operation → 1 slot less needed for compressed mode
- Ca. 1,5 years IP development efforts savings due to reduced integration efforts

New Partitioning for RF Data and Control through Digital Standard Interfaces



- Classical RF Engine system: BB controls RF Transceiver and FE-devices

  => Complex BB-RF-interface

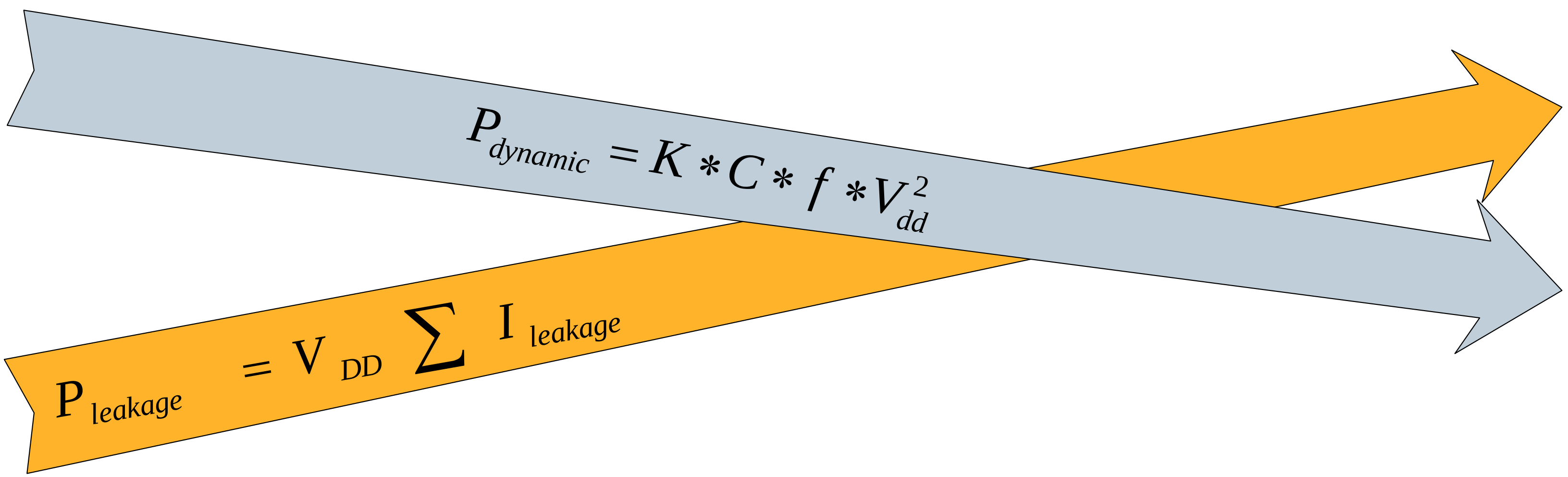


System advantage:

- Incorporated front end control for complete RF engine
- Complete RF sub-system is controlled by transceiver

Power Consumption Basics
The Effect of Technology

We have to follow technology to get always more integration and performances, minimizing the disadvantages



130 nm

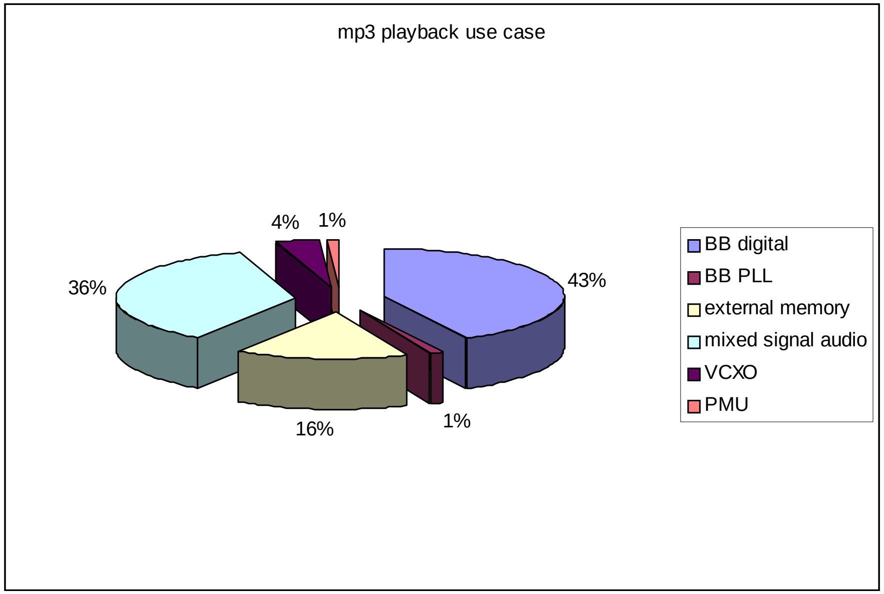
90 nm

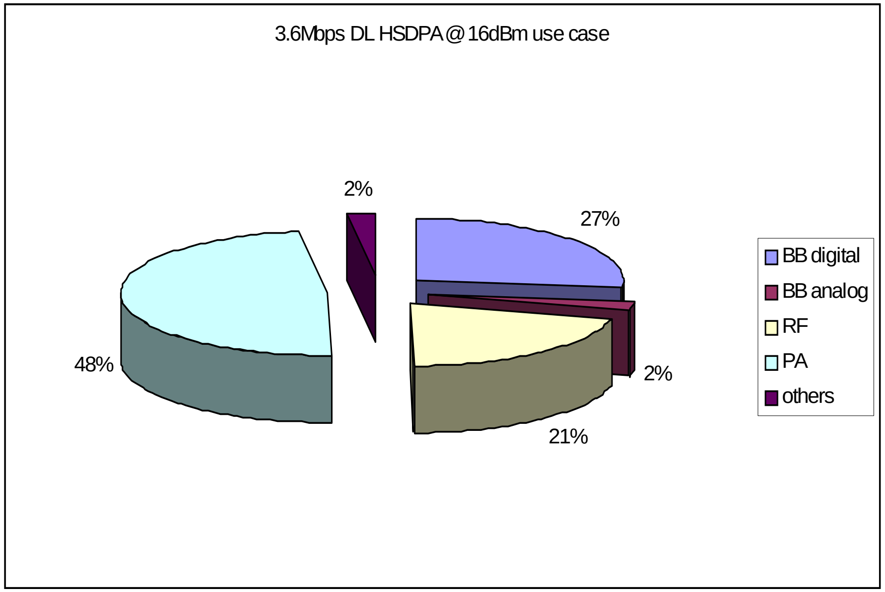
65 nm

Where Does the Power Go in Mobile Phones?

Typical mp3 playback use case (RF switched off)

Typical HSDPA use case



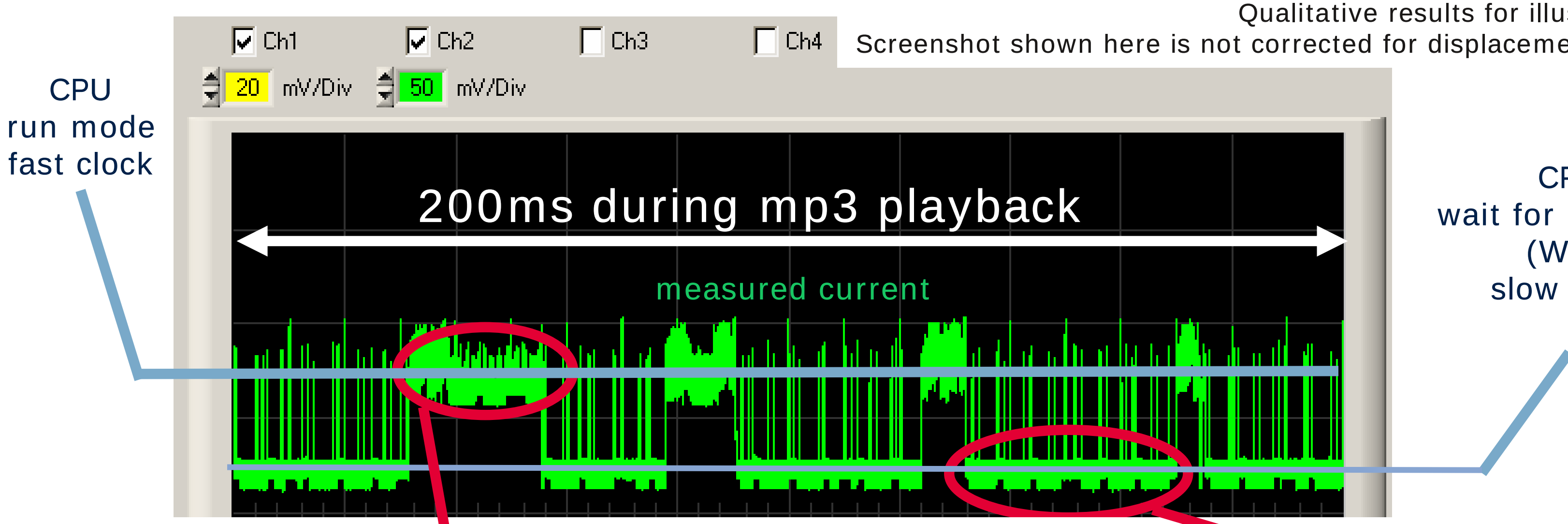


> 50% of the total power is consumed by digital baseband processor and memory

Digital baseband is a significant contributor even at high output power

Power Optimized Applications
Power Saving Features & Reduced Activity

Qualitative results for illustration only.
Screenshot shown here is not corrected for displacement of probes.



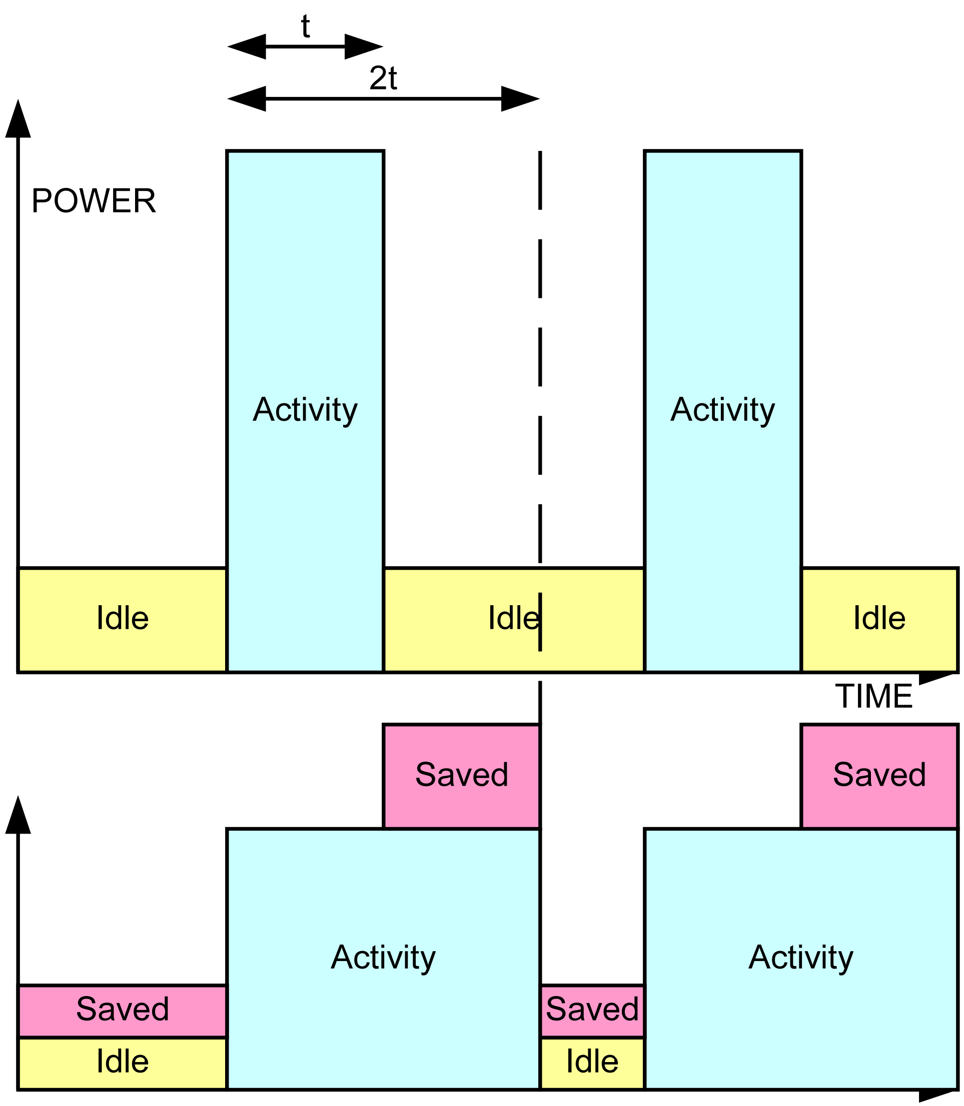
Reduce current in RUN mode

- Reduce CPU load
- → Lowest possible voltage and clock frequency
  Dynamic voltage and frequency scaling
- Switch off un-used peripherals
  Clock gating and/or power gating
- Minimize memory traffic

Reduce current in WFI mode

Reduce other system activities to the bare minimum

System and Use Case Know-How Allows Power Efficient Integration of Components



- Reducing the frequency reduces the wasted Idle time power
- In reality, often Activity is more reduced because of fixed time activity (e.g. memory accesses)
- Automatic clock reduction in idle mode is done in HW

Component-Based System Design Flow

High-level architecture

Definition of architecture principles and high-level system architecture

Component/ Subsystem architecture

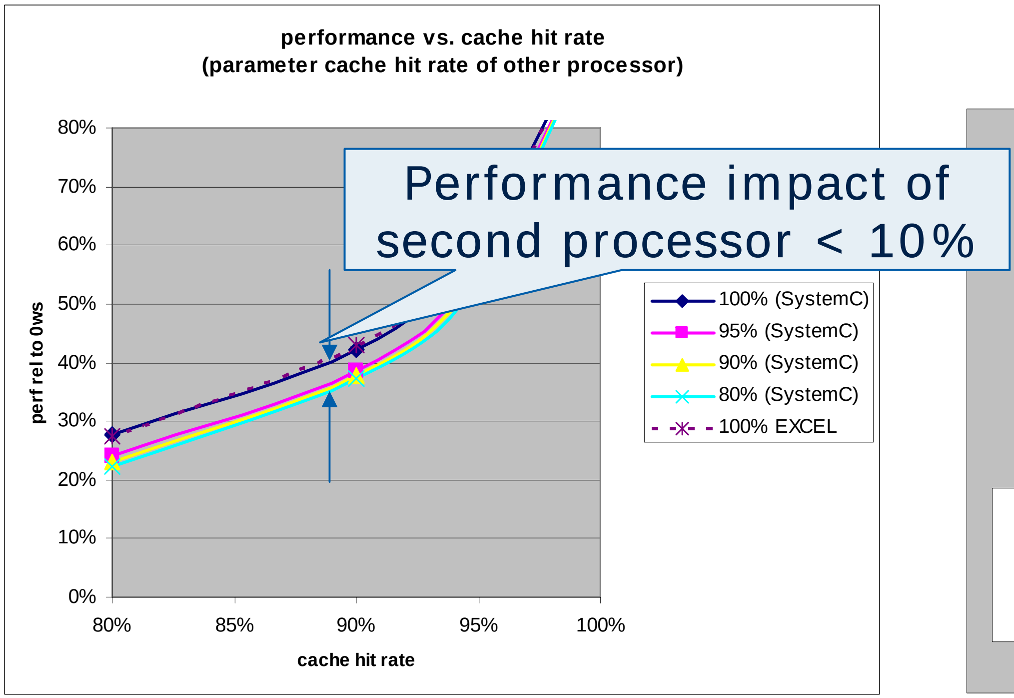
Efficient subsystem design
- Cost, power and performance optimized design
- HW/SW co-design
- Component-level model generation

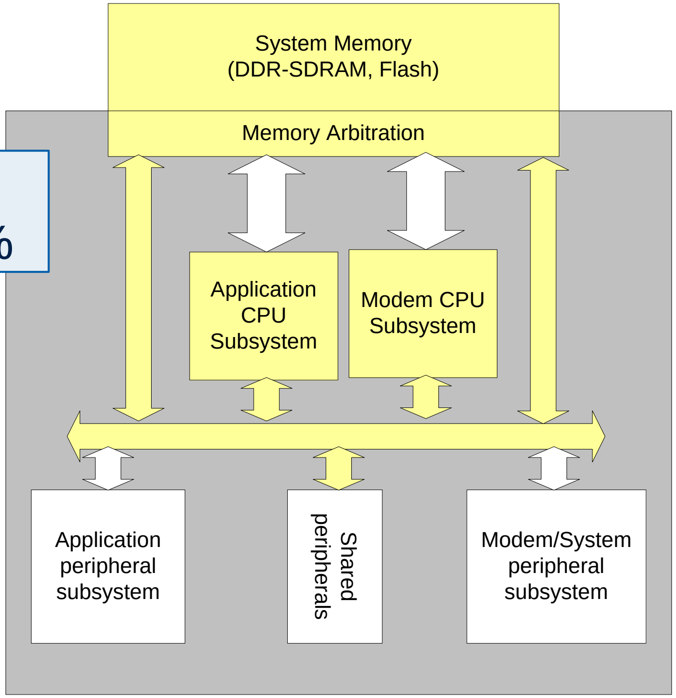
System integration

Integration on SoC platform with expensive resources shared

Verification task: check that integration does not affect the subsystem functionality

Example Design Task for Integration Component: Shared Memory Controller for 2 Processor Subsystems

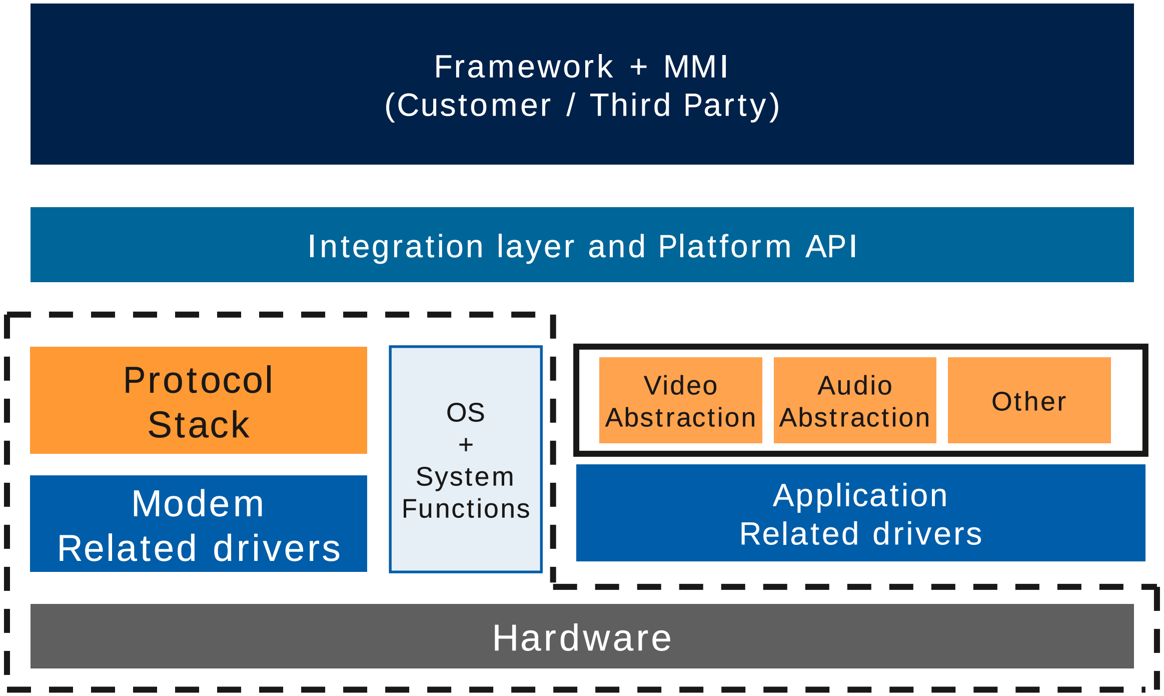


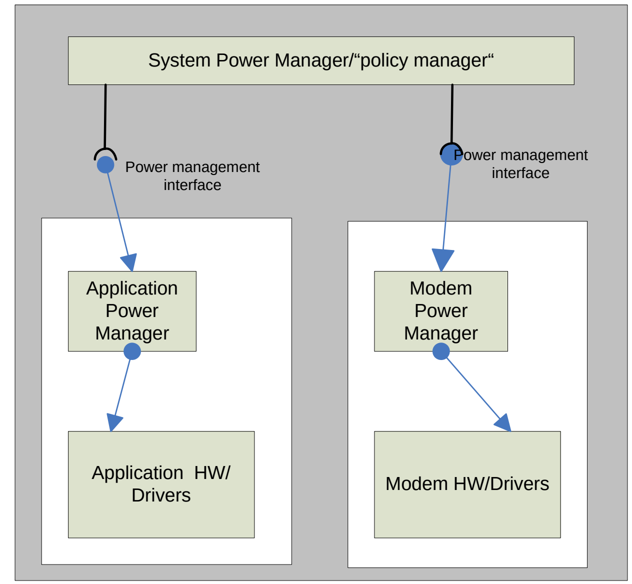


Processor cores share access to DRAM in a ping pong way

- ☑ Almost no performance interdependency of both subsystems
- ☑ Bandwidth also supports DMA processes

Operating Systems and Platform Service Components Serve as Integration Components on Shared Processors





- Distributed system control approach
  - Keep component related system control functions
  - system integration layer provides global system management components
- RTOS to manage integration of RT properties; must serve as integration component

- Components implement power management for self-managed policies
- Interface/API for global power policy control
- Termination and integration in overall platform through system power management component

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Summary and Conclusions

Feature complexity and integration are the main challenges

- The wireless market (for embedded systems) is becoming a consumer market and driven by expectations on user experience
- Devices have to integrate a multitude of features (each of them delivering the quality of a point consumer device) into one embedded system

Divide and conquer: Component based approach to handle complex features ✓

Divide-conquer-and-join: Seamless modelling, design and verification approach using integration components ?

Areas for Embedded Systems Research

Quality	Power consumption; User experience
Features	Multimedia; Display resolution; Audio; Interfaces
Design	Smaller form factors; Fashion
Scalability	Recognizable look and feel; Branding

Areas for Embedded Systems Research

Seamless modeling approaches for complex system behavior

Features

- Multimedia
- Display resolution
- Audio
- Interfaces

Design

- Smaller form factors
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Scalability

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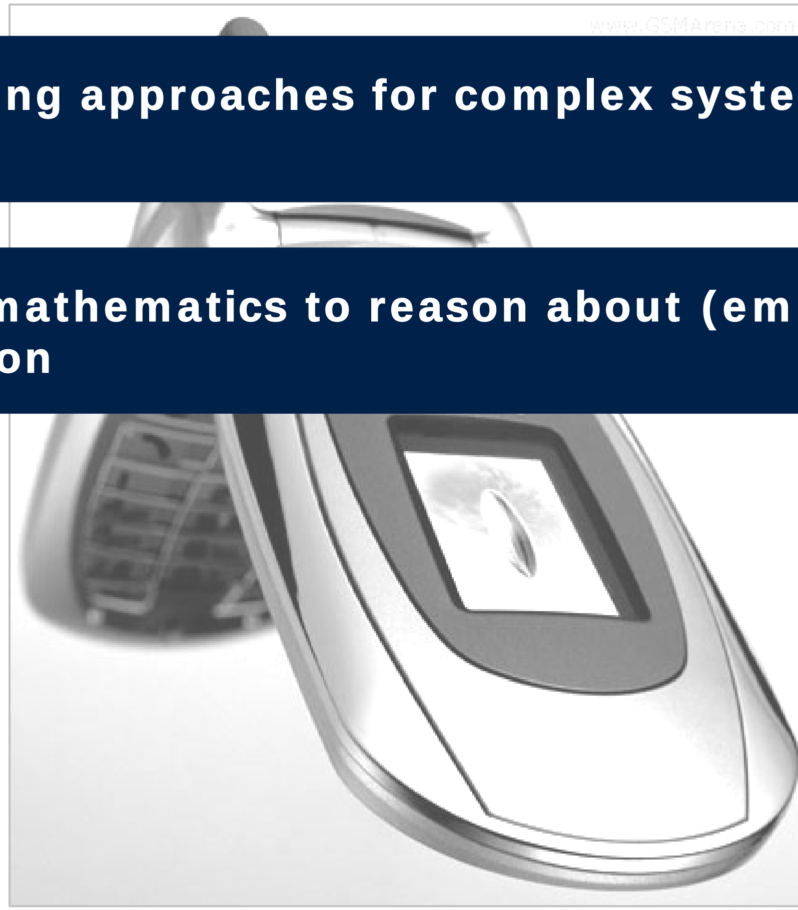
Areas for Embedded Systems Research

Seamless modeling approaches for complex system behavior

Languages and mathematics to reason about (embedded) system integration



Design

- Smaller form factors
- Fashion

Scalability

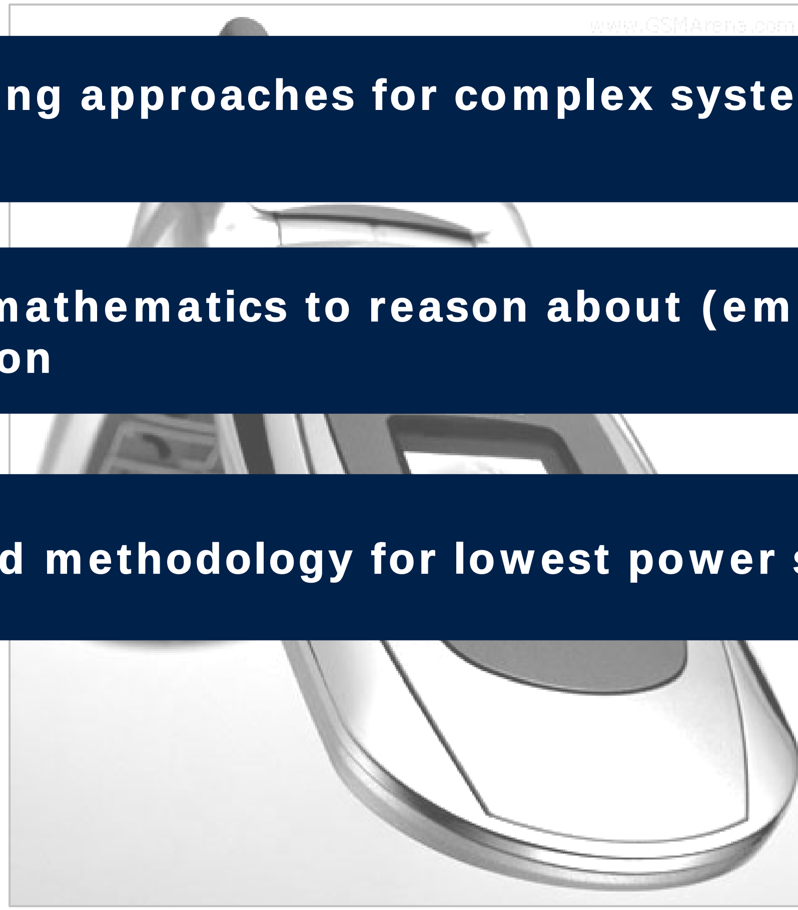
- Recognizable look and feel
- Branding

Areas for Embedded Systems Research

Seamless modeling approaches for complex system behavior

Languages and mathematics to reason about (embedded) system integration

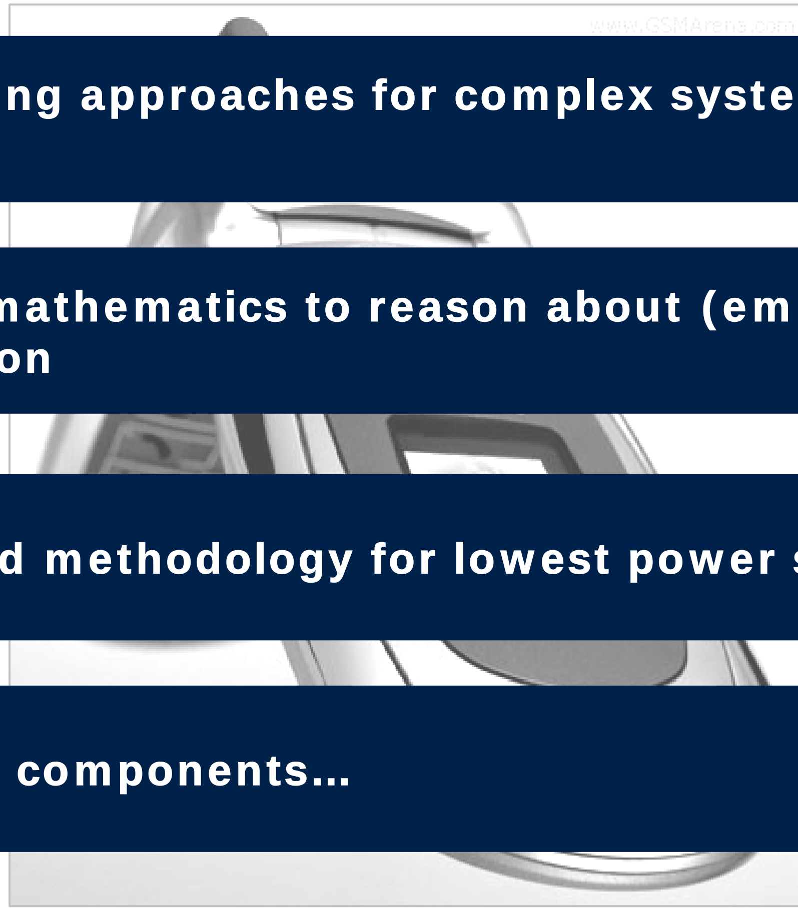
Architectures and methodology for lowest power systems



Scalability

- Recognizable look and feel
- Branding

Areas for Embedded Systems Research



Seamless modeling approaches for complex system behavior

Languages and mathematics to reason about (embedded) system integration

Architectures and methodology for lowest power systems

More integration components...

Never stop thinking