Complexity Challenges towards 4th Generation Communication Solutions

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Outline

- Introduction: Embedded Computing for Wireless Handhelds
- Embedded System Architecture Challenges
- Component-based Approach
- Summary and Conclusions
Introduction: Embedded Computing for Wireless Handhelds

Embedded System Architecture Challenges

Component-based Approach

Summary and Conclusions
Moving on to Multimedia Communication
Electronic Market
The Biggest Application is Mobile Telephony

Sold Pieces of selected Applications per Year (2005)

[Bar chart showing sold pieces of applications per year (2005)]

- **Mobile Phone**
- **Desktop PC**
- **DVD Player**
- **MP3 Player**
- **Digital Camera**
- **Laptop PC**
- **Set-top Box**
- **Game Console**

**Comment**

- Mobile phone segment is by far the largest segment for end user devices and thus a key market for embedded processing devices.

- Mobility and device convergence drive requirements for low power, computing performance and user experience.

*Source: CIBS World Markets Digital Media Bible March 2006*
Industrial Landscape

- €5,000bn
  - €1,100bn
    - €200bn
      - €50bn

- Telecom, Internet, Broadcast
- Consumer, Medical, Transport, Security, Space

Cornerstone of High-tech economy
Semiconductor Industry Size

[Graph showing the growth of the semiconductor industry from 1983 to 2009 with labeled cycles:
1. PC Cycle
2. PC/Windows Cycle
3. PC, Wireless, Asia Cycle

Source: WSTS, McClean Report 2006, UBS Primer]
Evolution of Asia’s Share in Electronic Equipment Manufacturing per Industry Segment

Source: Gartner
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The Evolution from GSM towards UMTS
UMTS - The Enabler for Real Wireless Multimedia

2nd Generation
- Data Rate: 9.6 kbps
- Applications: Voice, SMS
- Products: Phones

2.5th Generation
- Data Rate: 115 kbps, 384 kbps
- Applications: E-Mail, Data-Services
- Products: Smart Phones, PDAs

3rd Generation
- Data Rate: 384 kbps, 2 Mbps
- Applications: Multimedia Services, Interactive Games
- Products: Mobile Multimedia Terminals

“Historical” view
Few Simple Criteria Drive the Development of Mobile Handset Architectures

- Quality
- Features
- Design
- Scalability

- Power consumption
- User experience
- Multimedia
- Display resolution
- Audio
- Interfaces
- Smaller form factor
- Fashion
- Recognizable look and feel
- Branding
Feature Requirements are Getting More Complex

Growing number and complexity of mobile phone features needs to be handled in a structured way
Growing number and complexity of mobile phone features needs to be handled in a structured way
Mobile Device is Becoming an „All-In-One Solution“

- 3D Graphics
- DVD
- Spiders
- Security
- DSC
- Camera
- Video conferencing
- Audio
- UWB
- WiMAX
- WLAN
- Bluetooth
- HSDPA
- Music/MP3
- Gaming
Mobile Device is Becoming an „All-In-One Solution“

(Hard) Real-time requirements
- Wireless radio access
- Audio and UI processing
- Power management

Constraint resources
- Battery (low-)powered
- Limited processing performance
- Limited memory
- Limited space

Integration of multiple subsystems
Future Mobile Phone Content Limited by Board Space

3G Co-Processor
PMU
GSM BB Processor
SIM-Card
NOR-Flash
SD-RAM
FM-Radio
3G TRX
UMTS PA/Band 2
GSM/EDGE TRX
FEM
GSM/EDGE PA
UMTS PA/Band 1
UMTS PA/Band 5
NAND-Flash
Bluetooth Modem
WLAN
UWB
GPS
DVB
WiMax
Moore's Law: Ever Increasing VLSI Power

- GSM Modem
- GSM, GPRS, EDGE Modem + Application
- GSM+UMTS Modem
- GSM, UMTS HSDPA, Bluetooth, WLAN, GPS, DVB-H

- 1µ CMOS 50k Tr.
- 0.25µ CMOS 11M Tr.
- 0.18µ CMOS 40M Tr.
- nm CMOS 1B Tr.

Mobile Pentium (~10W)
Wireless Communication Systems

- **WLANs 54 Mbps**
- **WLANs 500 Mbps**
- **Mobile WLANs**

**Doubling Every 16 Months!**

- **WLANs 54 Mbps**
- **WLANs 500 Mbps**
- **Mobile WLANs**

**Bits per second**


- **2G**
- **3G**
- **4G**

- **Digital Voice**
- **Multimedia Messaging, Medium-Speed, Packet Data**
- **Broadband Multimedia, Broadcast Video, High-Speed Packet Data**

**3.9G = LTE**

**802.11g**

**802.11n**

**UWB**

**Bluetooth**

**WLANs 500 Mbps**

**3G**

**3.5G = HSPA**

**2G**

**Digital Voice**


**Wireless Communication Systems**

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The Algorithmic Driving Force

Algorithmic Complexity (Shannon’s Law)

Processor Performance (Moore’s Law)

Battery Capacity
The Algorithmic Driving Force

- **Algorithmic Complexity (Shannon’s Law)**
- **Processor Performance (Moore’s Law)**
- **Battery Capacity**

Timeline:
- 1980
- 1984
- 1988
- 1992
- 1996
- 2000
- 2004
- 2008
- 2012
- 2016
- 2020

Key Milestones:
- 1G
- 2G
- 3G

Capacity:
- 0.5M Tr.
- 11M Tr.
- 40M Tr.
- 1B Tr.
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Cellular Communication Systems

4G
- Software Defined Radio
- Cognitive Radio
- Virtual MIMO

3G
- Hardware Radio
- Base Station Antenna Diversity
- Mobile Station Antenna
- Single Antenna Systems

2G
- GSM 10 kb/s
- GPRS 115 kb/s
- EDGE 384 kb/s
- UMTS 384 kb/s
- HSPA 14 Mbp/s
- HSPA+ 40 Mbp/s
- LTE 100 Mbp/s

4G 1 Gb/s

500 nm 250 nm 130 nm 65 nm 32 nm 16 nm

- Divide and conquer approach:
  - Cluster subsystems with similar computing and real-time properties
- Challenge for the conqueror: Integration
General Modeling Approach

- **Virtual Prototype**
  - SW development
  - Architecture decisions

- **High Level Model**
  - Early performance estimates
  - Use case data
  - CPU load
  - Cache hit rates
  - Power data

- **Live Measurements**
  - System validation & optimization
  - Performance & power targets
  - Use case data
  - CPU load
  - Cache hit rates
  - Power data

- **Project life**
  - Begin to end
  - Begin to running system
  - Running system to end
Complex Behavior of New Mobile Standards Require Prototype Models

- 2.75G L1 Firmware
  - Scheduling according to timing analysis (clustering of periods, interrupt driven, non-pre-emptive)
  - Uses hardware accelerators
  - Communication scheme GSM slot based
  - Simple performance model
    - Overall processing power

- 3.5G L1 processing
  - Controls low level physical layer procedures
  - Several HW accelerators involved
  - RTOS based implementation
  - Model generated through tracing and virtual prototyping
    - Event statistics
Complex Behavior of New Mobile Standards Require Prototype Models

- 2.75G L1 Firmware
  - Scheduling according to timing analysis (clustering of periods, interrupt driven, non-pre-emptive)

**Deterministic real time scheduling**
- Based
- Simple performance model
  - Overall processing power

- 3.5G L1 processing
  - Controls low level physical layer procedures
  - **Complex timing scenarios**
    - RTOS based implementation
    - Model generated through tracing and virtual prototyping
    - Event statistics

**AMR FULLRATE**
- Handsfree + Noise Reduction

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3.5G L1 processing
- Controls low level physical layer procedures
- **Complex timing scenarios**
- RTOS based implementation
- Model generated through tracing and virtual prototyping
- Event statistics
HSUPA Timing Diagram (Simplified)

Loop: Air ➔ L1 ➔ L2 ➔ L1 ➔ Air

- AGCH decoding (RAKE):
  - < 1.2 slots

- RGCH decoding (RAKE):
  - < 1.2 slots

- HICH decoding (DSP):
  - < 1.2 slots

- Physical Layer Rx:
  - E-DCH scheduling
  - TTI = 2ms worst case timing

- Link Layer:
  - MAC triggered by slot periodic INT
  - Encoding task started slot periodic context

- UL physical channel timing for TTI=2ms
  - 2 ms

- (N) sl. 1 (N) sl. 2 (N) sl. 3 (N+1) sl. 1 (N+1) sl. 2 (N+1) sl. 3 (N+2) sl. 1 (N+2) sl. 2 (N+2) sl. 3

- L2 MAC/RLC SW (μC)
  - L2 MAC / RLC HW (PS-Processor)
  - TrBks (N-2)
  - TrBks (N-1)
  - TrBks (N)

- E-DCH Encoding
  - TrBks (N-2)
  - TrBks (N-1)
  - TrBks (N)

- Modulator
  - (N-3) sl. 2 (N-3) sl. 3 (N-2) sl. 1 (N-2) sl. 2 (N-2) sl. 3 (N-1) sl. 1 (N-1) sl. 2 (N-1) sl. 3 (N) sl. 1 (N) sl. 2 (N) sl. 3 (N+1) sl. 1 (N+1) sl. 2 (N+1) sl. 3

- 1024 chips = 40.4 slot
- ~256 chips = 0.1 slot
- < 1 slot E-DCH @ Cat4, 2ms

- worst case: 3.6 ms
HSUPA Timing Diagram (Simplified)

Loop: Air → L1 → L2 → L1 → Air

Parallelization + Multi-threading + Pipelining
LTE
Physical Layer Complexity (4x4 Configuration)

Jens Berkmann
2006-12-07
Version 0.1

100 C-MIPS 100 C-MIPS

640 C-MIPS 1340 C-MIPS 1024 MIPS 6144 MIPS 160 MIPS

Optional IC Loop — Depending on #Codewords

Interference Cancellation
Re-Modulation
Interleaving
Rate Matching
Turbo Encoding

Spatial Equalizer
& Spatial Time/Freq Combiner

DeRateMatching Viterbi Decoding UE Detection

LLR

Data

HARQ Processing
DeRateMatching Turbo Decoding

Ctrl Data

CQI

CRC

ACK/NACK

780 C-MIPS

2000 MIPS

Precoding Matrix Determination & Rank Adaptation

Precoding Index

Channel Rank

ChEst Rx1

ChEst Rx2

ChEst Rx3

ChEst Rx4

Cell Search

Cell Info

# Tx Antennas
Programmable Baseband Processor

- 90nm CMOS
- Multi-Mode Capability
- Scalable by adding MACs ALUs Memories Accelerators
- Low Power Architecture

MT SIMD = multi tasking, single instruction, multiple data
RF - Challenges

- Cover Frequency Band up to 77 GHz
  - Highly selective filters for many bands needed
    - "Frontend Challenge"

- Flexible Reconfigurable High Performance Radio
  - Multiple Radios on One Chip
  - Multi-band RF engines (complex control scenarios)
  - MIMO Systems (demanding control loops)
    - "Multi-Mode/Multi-Band Challenge"

- Electromagnetic Design on Chip
  - “Power-Amplifier Challenge”

- RF SoC Design and Simulation Methodology
  - “Complexity & Verification Challenge”
State-of-the-Art Analog DCR Architecture

- Analog channel selection
- Analog IQ interface
- Technology for the BB-IC needs to have an analog option
Channel selection moved to the digital domain
Increased ADC requirements
RF impairment correction in the digital domain
## Approach

- Multimode and Multi-standard topics
  - RF front-end control complexity
  - High load on BB to close control loops
  - Link of RF and BB innovation

- Approach: Move some RF-related baseband processing functions into transceiver

- Results in autonomous RF engine design

## Benefits

- Platform development in shorter time and reduced costs (SW development savings)

- Reduced production line calibration time and investment needed (ca. 20%)

- Improved System performance e.g: Faster IRAT operation → 1 slot less needed for compressed mode

- Ca. 1,5 years IP development efforts savings due to reduced integration efforts
New Partitioning for RF Data and Control through Digital Standard Interfaces

- **System advantage:**
  - Incorporated front end control for complete RF engine
  - Complete RF sub-system is controlled by transceiver

- **Classical RF Engine system:**
  - BB controls RF Transceiver and FE-devices
  - => Complex BB-RF-interface
We have to follow technology to get always more integration and performances, minimizing the disadvantages.

\[ P_{\text{dynamic}} = K \cdot C \cdot f \cdot V_{dd}^2 \]

\[ P_{\text{leakage}} = V_{DD} \sum I_{\text{leakage}} \]

130 nm  90 nm  65 nm
Where Does the Power Go in Mobile Phones?

Typical mp3 playback use case
(RF switched off)

Typical HSDPA use case

> 50% of the total power is consumed by digital baseband processor and memory

Digital baseband is a significant contributor even at high output power
Power Optimized Applications
Power Saving Features & Reduced Activity

Qualitative results for illustration only. Screenshot shown here is not corrected for displacement of probes.

- Reduce current in RUN mode
  - Reduce CPU load
  - Lowest possible voltage and clock frequency
    Dynamic voltage and frequency scaling
  - Switch off un-used peripherals
    Clock gating and/or power gating
  - Minimize memory traffic

- Reduce current in WFI mode

- Reduce other system activities to the bare minimum

CPU run mode fast clock
CPU wait for interrupt (WFI) slow clock
System and Use Case Know-How Allows Power Efficient Integration of Components

- Reducing the frequency reduces the wasted Idle time power
- In reality, often Activity is more reduced because of fixed time activity (e.g. memory accesses)
- Automatic clock reduction in idle mode is done in HW
Component-Based System Design Flow

High-level architecture

Definition of architecture principles and high-level system architecture

Efficient subsystem design
- Cost, power and performance optimized design
- HW/SW co-design
- Component-level model generation

Component/Subsystem architecture

System integration

Integration on SoC platform with expensive resources shared

Verification task: check that integration does not affect the subsystem functionality
Example Design Task for Integration Component:
Shared Memory Controller for 2 Processor Subsystems

Performance impact of second processor < 10%

Processor cores share access to DRAM in a ping pong way
☑  Almost no performance interdependency of both subsystems
☑  Bandwidth also supports DMA processes
Operating Systems and Platform Service Components Serve as Integration Components on Shared Processors

- Distributed system control approach
  - Keep component related system control functions
  - System integration layer provides global system management components
- RTOS to manage integration of RT properties; must serve as integration component

- Components implement power management for self-managed policies
- Interface/API for global power policy control
- Termination and integration in overall platform through system power management component
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Summary and Conclusions

Feature complexity and integration are the main challenges

- The wireless market (for embedded systems) is becoming a consumer market and driven by expectations on user experience
- Devices have to integrate a multitude of features (each of them delivering the quality of a point consumer device) into one embedded system

Divide and conquer: Component based approach to handle complex features

Divide-conquer-and-join: Seamless modelling, design and verification approach using integration components
Areas for Embedded Systems Research

- Quality
- Features
- Design
- Scalability

Quality:
- Power consumption
- User experience

Features:
- Multimedia
- Display resolution
- Audio
- Interfaces

Design:
- Smaller form factors
- Fashion

Scalability:
- Recognizable look and feel
- Branding
Areas for Embedded Systems Research

Seamless modeling approaches for complex system behavior

- Features
- Design
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Areas for Embedded Systems Research

Seamless modeling approaches for complex system behavior

Languages and mathematics to reason about (embedded) system integration

Design

Scalability

- Smaller form factors
- Fashion
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Areas for Embedded Systems Research

- Seamless modeling approaches for complex system behavior
- Languages and mathematics to reason about (embedded) system integration
- Architectures and methodology for lowest power systems

Scalability
- User experience
- Power consumption
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Areas for Embedded Systems Research

Seamless modeling approaches for complex system behavior

Languages and mathematics to reason about (embedded) system integration

Architectures and methodology for lowest power systems

More integration components...
We commit.
We innovate.
We partner.
We create value.