Monday, October 1st - 10.30 - 12.00

1. **Simultaneous Synthesis of Buses, Data Mapping and Memory Allocation for MPSoC**
   *Brett H. Meyer and Donald E. Thomas*

2. **A Framework for Rapid System-level Exploration, Synthesis, and Programming of Multimedia MP-SoCs**
   *M. Thompson, H. Nikolov, T. Stefanov, A.D. Pimentel, C. Erbas, S. Polstra and E. Deprettere*

3. **Predictable Execution Adaptivity through Embedding Dynamic Reconfigurability into Static MPSoC Schedules**
   *Chengmo Yang and Alex Orailoglu*

Monday, October 1st - 01.30 - 03.30

1. **Synchronization after Design Refinements with Sensitive Delay Elements**
   *Tarvo Raudvere, Ingo Sander, Axel Jantsch*

2. **Embedded Software Development on top of Transaction-Level Models**
   *Wolfgang Klingauf, Robert Günzel, Christian Schröder*

3. **Pointer Re-coding for Creating Definitive MPSoC Models**
   *Pramod Chandraiah, Rainer Doemer*

Monday, October 1st - 04.00 - 05.30

1. **Energy Efficient Hardware-Software Co-scheduling in Dynamically Reconfigurable Systems**
   *Pao-Ann Hsiung and Chih-Wen Liu*

2. **Dynamic Synthesis of Thread Accelerators**
   *Greg Stitt, Frank Vahid*

3. **HW/SW Co-Design for Reactive Processing**
   *Sascha Gärdtke, Claus Traulsen, Reinhard von Hanxleden*

3B: Low Power Design and Thermal Control

1. **Power Deregulation: Eliminating Off-Chip Voltage Regulation Circuitry From Embedded Systems**
   *Seunghoon Kim, Robert P. Dick, and Russ Joseph*

2. **Temperature-Aware Processor Frequency Assignment for MPSoCs Using Convex Optimization**
   *Srinivasan Murali, Almir Mutapcic, David Atienza, Rajesh Gupta, Stephen Boyd, Giovanni De Micheli*

3. **Three-Dimensional Multi-Processor System-on-Chip Thermal Optimization**
   *Sun Chong, Li Shang, and Robert P. Dick*
Tuesday, October 2nd - 09.00 - 10.00

Keynote moderated by Professor Juergen Teich
1. Complexity Challenges towards 4th Generation Communication Solutions
   Professor Hermann Eul, Infineon, Germany

Tuesday, October 2nd - 10.30 - 12.00

Special Session I, Organizer Sri Parameswaran

Tuesday, October 2nd - 01.30 - 03.30

4A: Embedded Software
1. Memory Access Optimization of Regular Loop-Nests in Wireless
   Javed Absar, Min Li, Praveen Raghavan, Andy Lambrechts, Murali Jayapala, Francky Cathoor, Arnout Vandecappelle
2. A Code-Generator Generator for Multi-Output Instructions
   Hanno Scharwaechter, Rainer Leupers, Heinrich Meyr, Jonghee Youn, Yunheung Paek
3. Influence of Procedure Cloning on WCET Prediction
   Paul Lokuciejewski, Heiko Falk, Martin Schwarzer, Peter Marwedel
4. Compile-Time Decided Instruction Cache Locking Using Worst-Case Execution Paths
   Heiko Falk, Sascha Plazar, Henrik Theiling

4B: Advances in NoC Optimization
1. Channel Trees: Reducing Latency by Sharing Time Slots in Time-Multiplexed Networks on Chip
   Andreas Hansson (Eindhoven University of Technology), Martijn Coenen (Corporate Research Department NXP Semiconductors), Kees Goossens (Corporate Research Department NXP Semiconductors, Delft University of Technology)
2. Performance and Resource Optimization of NoC Router Architecture for Master and Slave IP Cores
   Glenn Leary, Krishna Mehta, and Karam S. Chatha
3. Incremental Run-time Application Mapping for NoCs with Multiple Voltage/Frequency Domains
   Chen-Ling Chou, Radu Marculescu
4. A Data Protection Unit for NoC-based Architectures
   Leandro Fiorin, Gianluca Palermo, Slobodan Lukovic, Cristina Silvano

Tuesday, October 2nd - 04.00 - 05.30

5A: System-Level Performance Analysis
1. Complex Task Activation Schemes in System Level Performance Analysis
   Wolfgang Haid and Lothar Thiele
2. Exact Response Time Analysis of Tasks Scheduled under Preemptive Round Robin
   Razvan Racu and Li Li and Rafik Henia and Arne Hamann and Rolf Ernst
3. A Hybrid Approach for Performance Risk Analysis at System-Level
   Alexander Viehl, Markus Schwarz, Oliver Bringmann, Wolfgang Rosenstiel

5B: Case Studies and Emerging Techniques
1. ESL Design and HW/SW Co-verification of High-end Software Defined Radio Platforms
   Ng, A. C.H., Weijers, J.W., Glassee, M., Schuster, T., Bougard, B., Van der Perre, L.
2. Smart Driver for Power Reduction in Next Generation Bi-Stable Electrophoretic Display Technology
   Michael A. Baker, Dr. Aviril Shrivastava, Dr. Karamvir Chatha
3. On the Impact of Manufacturing Process Variations on the Lifetime of Sensor Networks
   Siddharth Garg and Diana Marculescu

Wednesday, October 3rd - 10.30 - 12.00

Special Session II, Organizer Sri Parameswaran

Wednesday, October 3rd - 01.30 - 03.00

6A: System-Level Synthesis
1. **A Low Power VLIW Processor Generation Method by Means of Extracting Non-redundant Activation Conditions**  
   Hirofumi Iwato, Keishi Sakanushi, Yoshinori Takeuchi, and Masaharu Imai

2. **Scheduling and Voltage Scaling for Energy/Reliability Trade-offs in Fault-Tolerant Time-Triggered Embedded Systems**  
   Paul Pop, Kåre Harbo Poulsen, Viacheslav Izosimov, Petru Eles

3. **Reliable Multiprocessor System-On-Chip Synthesis**  
   Changyun Zhu, Zhenyu Gu, Robert P. Dick, and Li Shang

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**6B: Embedded Systems Architecture**

1. **Aggressive Snoop Reduction for Synchronized Producer-Consumer Communication in Energy-Efficient Embedded Multi-Processors**  
   Chenjie Yu, Peter Petrov

2. **Predator: A Predictable SDRAM Memory Controller**  
   Benny Akesson (Technische Universiteit Eindhoven), Kees Goossens (NXP Research and Delft University of Technology) and Markus Ringhofer (Graz University of Technology)

3. **Performance Improvement of Block Based NAND Flash Translation Layer**  
   Siddharth Choudhari, Tony Givargis

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**Wednesday, October 3rd - 15.30 - 16.30**

Panel, responsible Adam Donlin

Contact [administrator](mailto:admin@codes-isss.org) for comments/questions