Board / System Level DFT

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Design for Test

- Testability: measure of costs in testing
- Major factors in test generation cost
  - Controllability
  - Observability
  - Predictability
- Lower costs by increasing testability

Levels of Abstraction

- Gate level
- Register-transfer level (RTL)
- Board level
- System level
  - What is a system?
    - Several boards
    - SoC
    - Hardware + software

Outline

- RTL level DFT techniques
  - Advanced scan concepts
    - Multiple test session
    - Partial scan using I-paths
    - Structured partial scan design
- Board/system-level DFT techniques
  - System-level busses
  - System-level scan paths
  - Boundary-scan standards
    - IEEE 1149.1
- Discussion

Multiple Test Session, 1

- Scan-based DFT technique at RTL level
- Test session
  - Configuring the scan paths and logic for testing
  - Testing using the scan-test methodology
  - Parameters
    - Number of test patterns
    - Number of shifts for each pattern
- Idea
  - reduce test application time by having several **(multiple) test sessions**

Multiple Test Session, 2

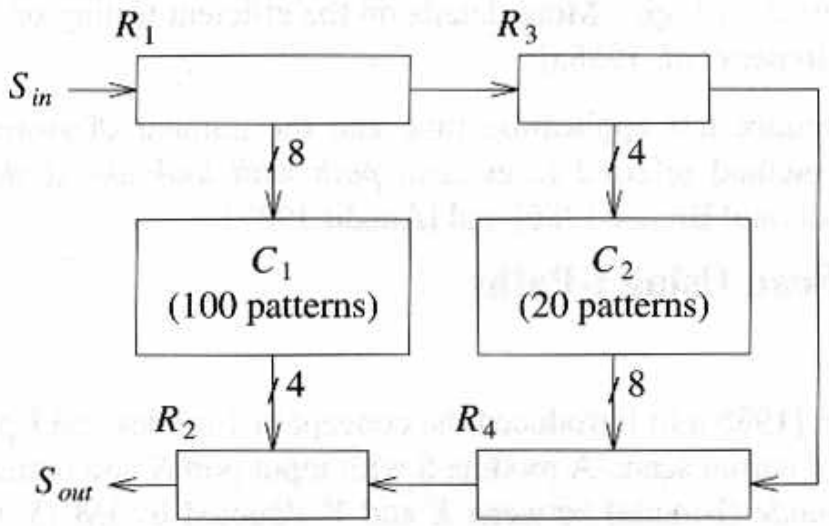


Figure 9.36 Testing using multiple test sessions

- Three modes
  - Together
    - 100x12=**1200** clock cycles
  - Separate
    - C_1: 100x8=800
    - C_2: 20x8=160
      - Scan paths need reconfiguring
    - Total: **960**
  - Overlapped
    - C_1 and C_2: 12x20=240
    - Rest of C_1: 80x8=640
    - Total: **880**
- No ranking among techniques

BALLAST: A Structured Partial Scan Design

- Scan-based DFT technique at RTL level
- Trade-off
  - ATG cost / performance
  - Adding storage cells to the scan path will reduce ATG computation

- BALLAST: Balanced Structure Scan Test
  - Method to select a subset of storage cells as part of the scan path
  - The resulted circuit must be **balanced** (still **sequential**)
  - Only **combinatorial** ATG is required

BALLAST: Circuit Model, 1

- Sequential circuit *S*
  - Blocks of combinatorial logic
    - Interconnected
    - Register
      - Collection of one or more storage cells
  - Partitioned into **clouds**

- Cloud
  - Maximal regions of connected combinatorial logic
  - Clouds can be **vacuous** or **nonvacuous**

BALLAST: Circuit Model, 2

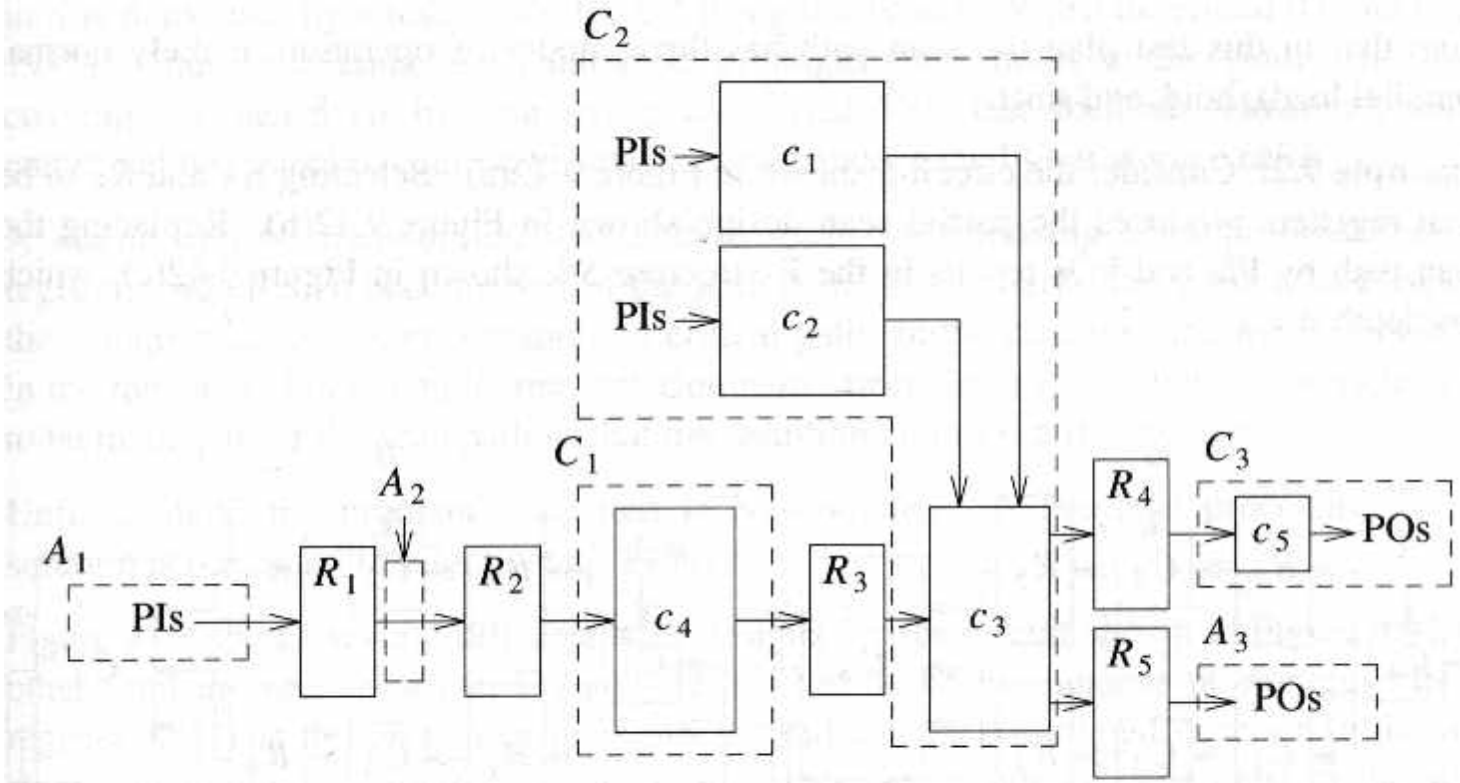


Figure 9.40 A partitioned circuit showing clouds and registers

BALLAST: Circuit Model, 3

- Cloud
  - Inputs
    - Primary inputs
    - Outputs of storage cells
  - Outputs
    - Primary outputs
    - Inputs to storage cells

- A group of wires is a **vacuous cloud**, if
  - Outputs of one register -> inputs of another, **or**
  - Circuit primary inputs -> inputs of a register, **or**
  - Outputs of a register -> primary outputs

BALLAST: Balanced Circuit

- *S* is **balanced** if ? v_1, v_2 ? *S*
  all signal paths (if any) between v_1 and v_2 go through the same number of registers
  - *S* is a sequential circuit
  - v_1 and v_2 are clouds
  - *S* must have an acyclic structure

- The circuit on slide 9 is balanced
- The circuit on slide 12 is non-balanced

BALLAST: Non-balanced Circuits

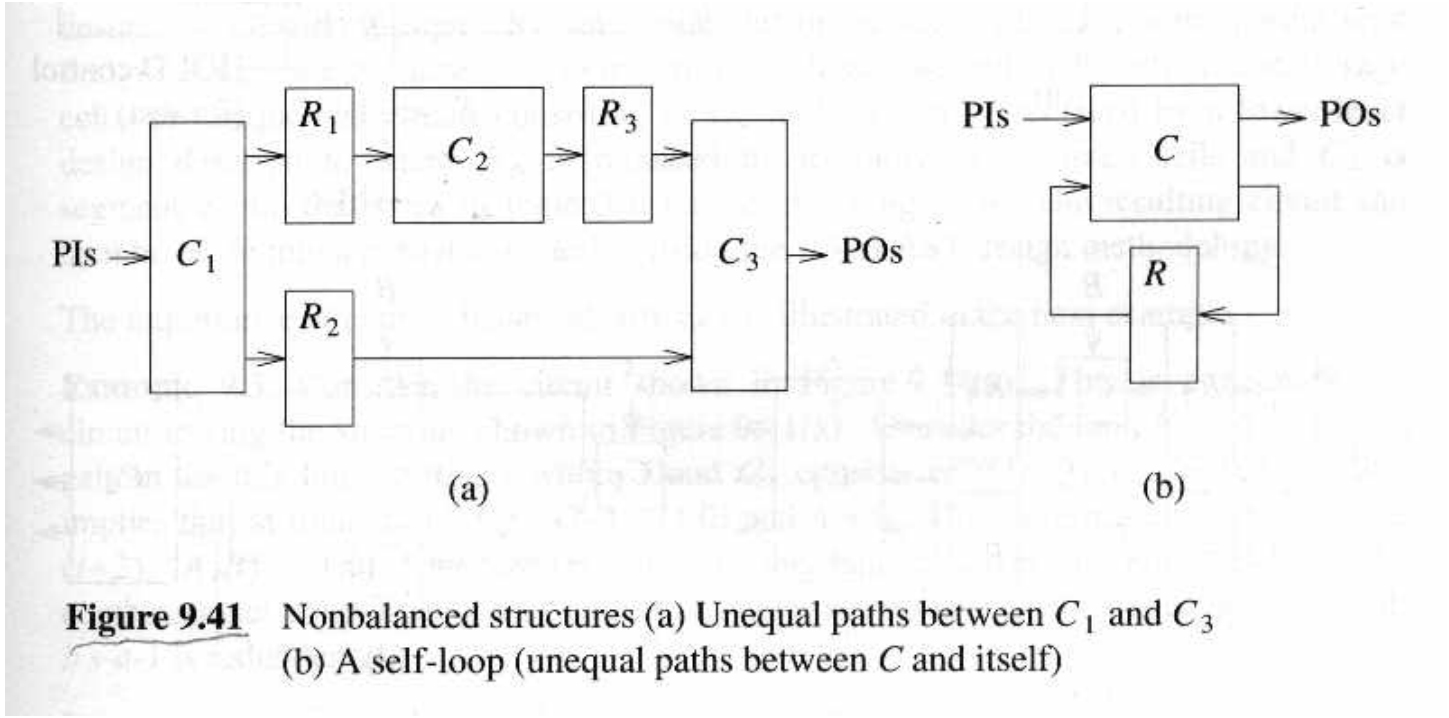
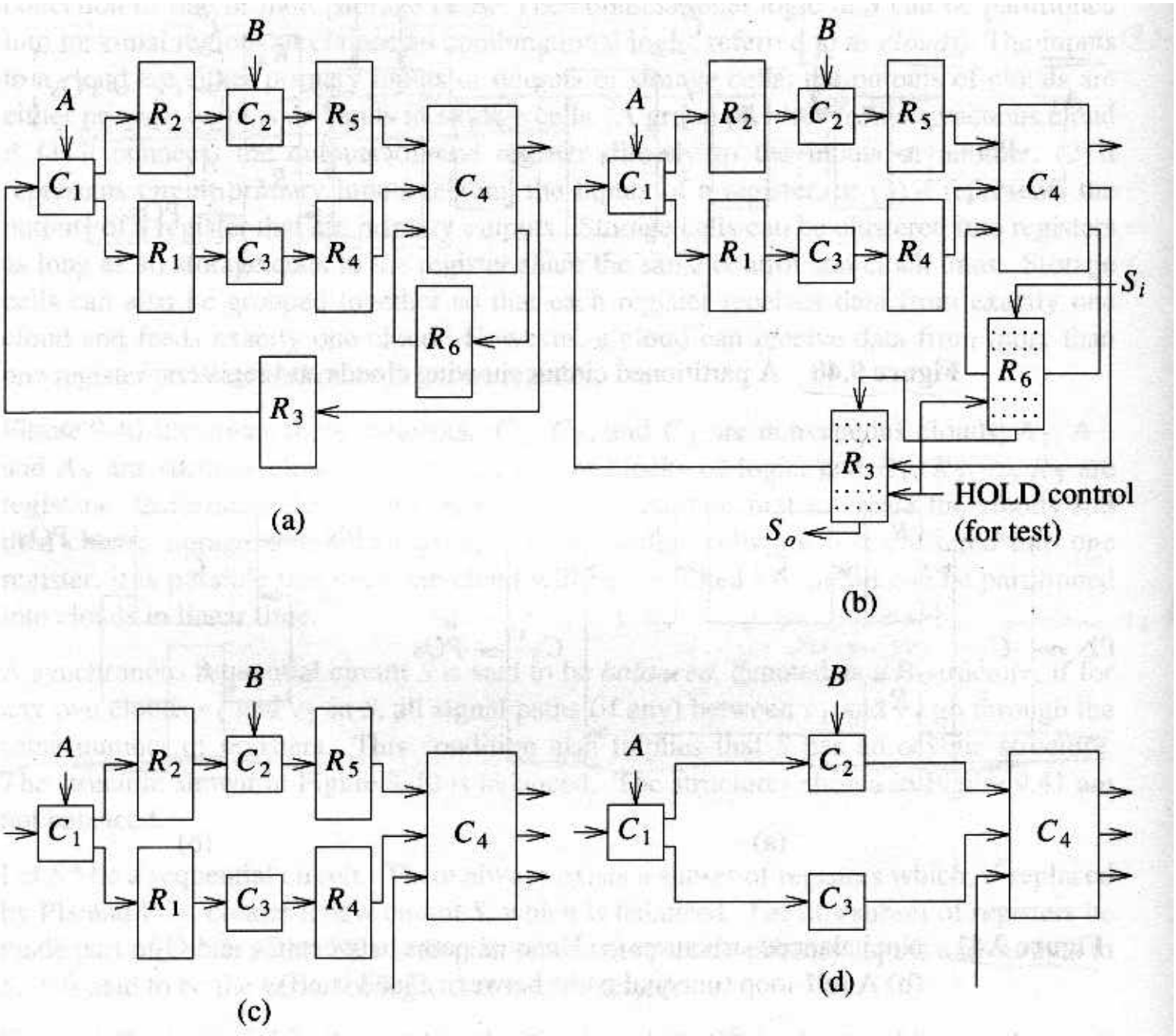


Figure 9.41 Nonbalanced structures (a) Unequal paths between C_1 and C_3 (b) A self-loop (unequal paths between C and itself)

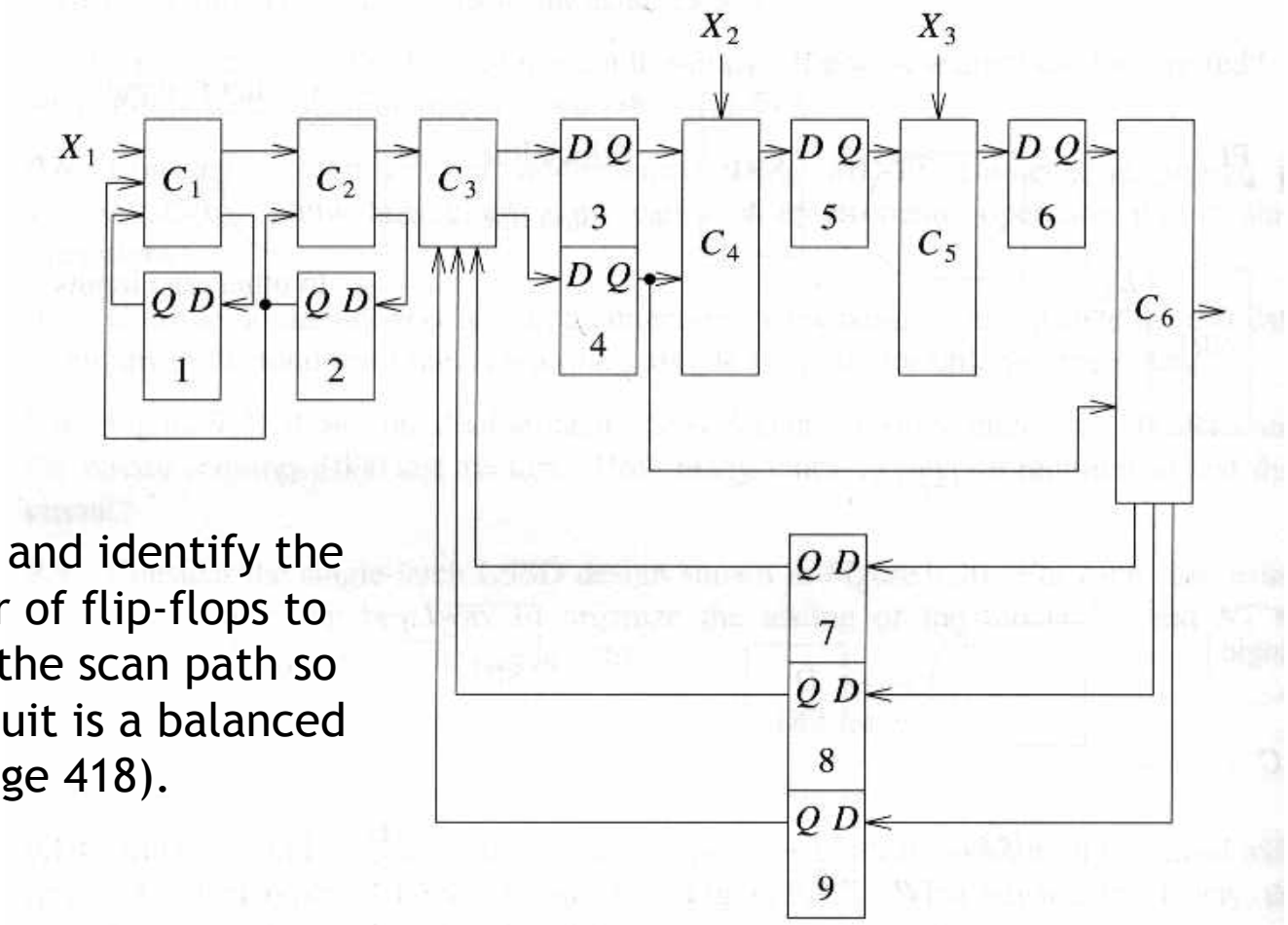
BALLAST's Idea

- Each **balanced sequential** circuit *S* has a **combinatorial** equivalent *C*
  - Obtained by replacing each storage cell in *S* by a wire
- All faults that can be detected in *S* are detectable by a test vector for *C*
  - Sollution: ATG only for *C*

- Transforming *S* into a balanced circiuit is NP
  - Heuristic from Gupta et al. 1989
    - Removing registers which will become part of the scan path
    - Minimal number of storage cells


A
B
C_1
C_2
C_3
C_4
R_1
R_2
R_3
R_4
R_5
R_6
(a)
S_i
S_o
HOLD control
(for test)
(b)
(c)
(d)

Problem



- Cloud the circuit and identify the minimum number of flip-flops to be made part of the scan path so the resulting circuit is a balanced structure (see page 418).

System-level Busses,1

- System
  - Collection of PCBs
  - PCB collection of ICs
- Functional testing
  - The functional system bus is used to control and observe signals
  - ATE takes control of the buses
  - Complex, manually generated functional tests

System-level Busses,2

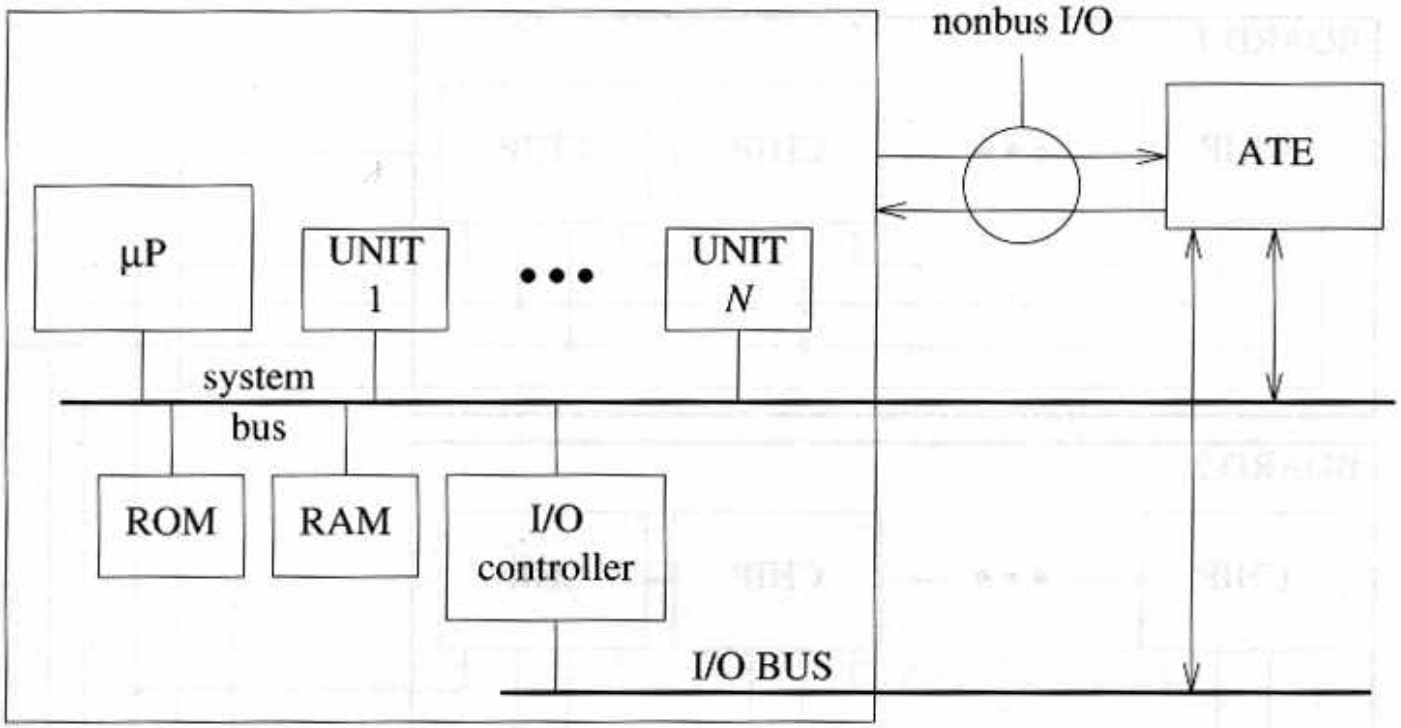


Figure 9.34 System-level test using system bus

Circuit-level Scan Paths

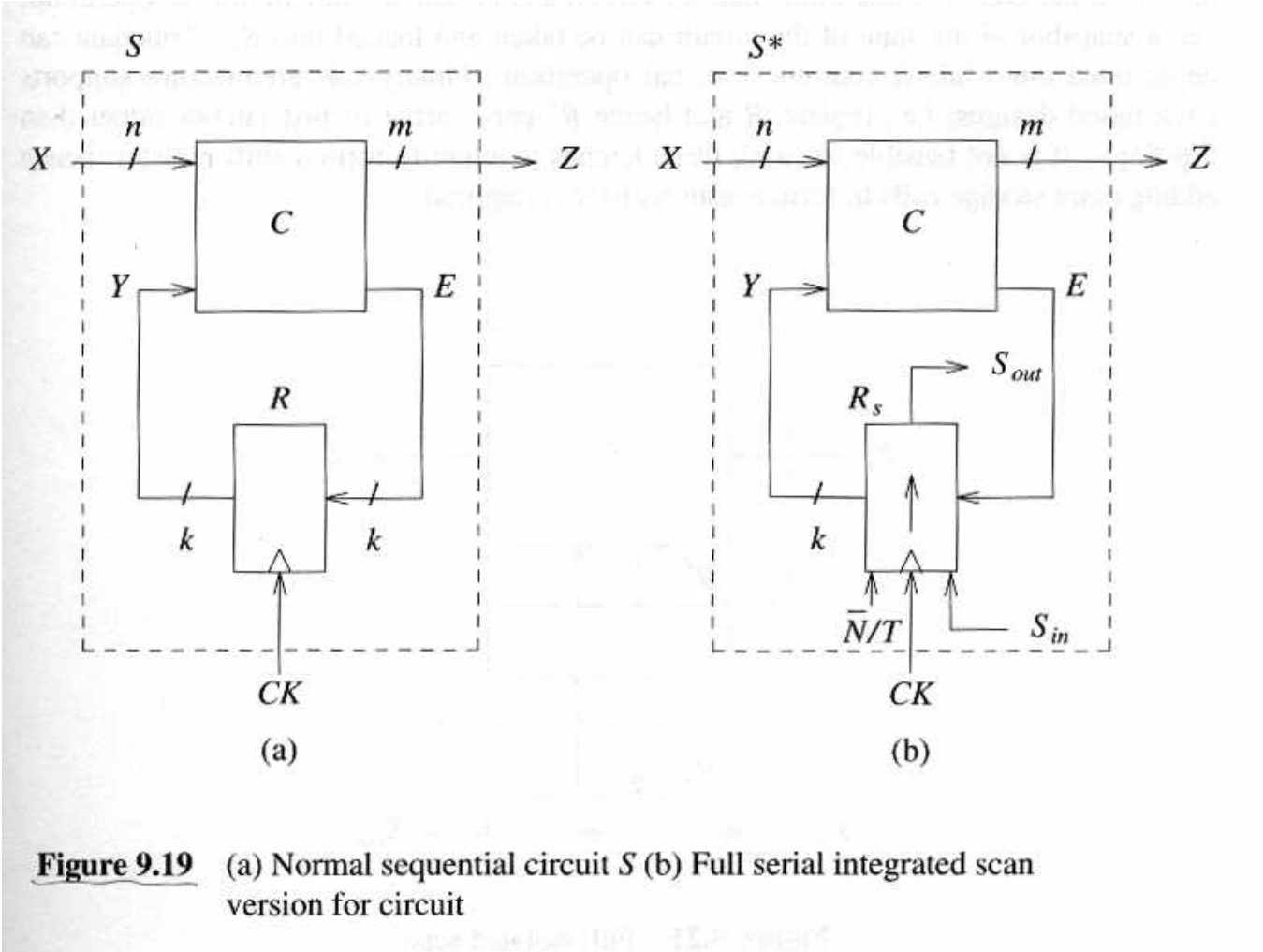


Figure 9.19 (a) Normal sequential circuit *S* (b) Full serial integrated scan version for circuit

System-level Scan Paths, 1

- System
  - Collection of PCBs
  - PCB collection of ICs
- Scan paths
  - Board scan path: ICs in a daisy chain
  - System scan path: boards interconnected
    - Common S_{in}, $\overline{N}/T$ and CK
    - S_{out} wired together

System-level Scan Paths, 2

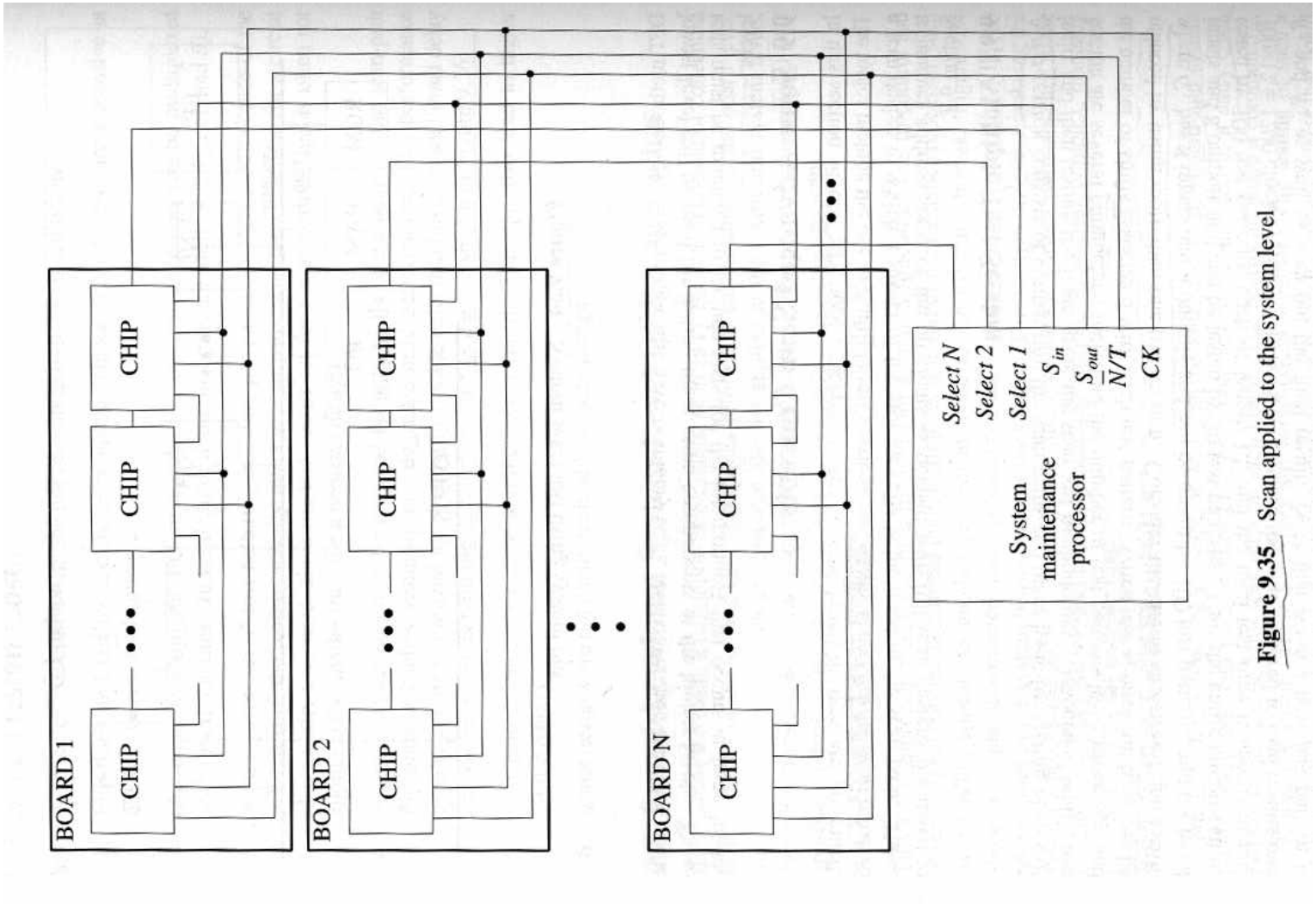


Figure 9.35 Scan applied to the system level

Circuit-level Boundary-scan

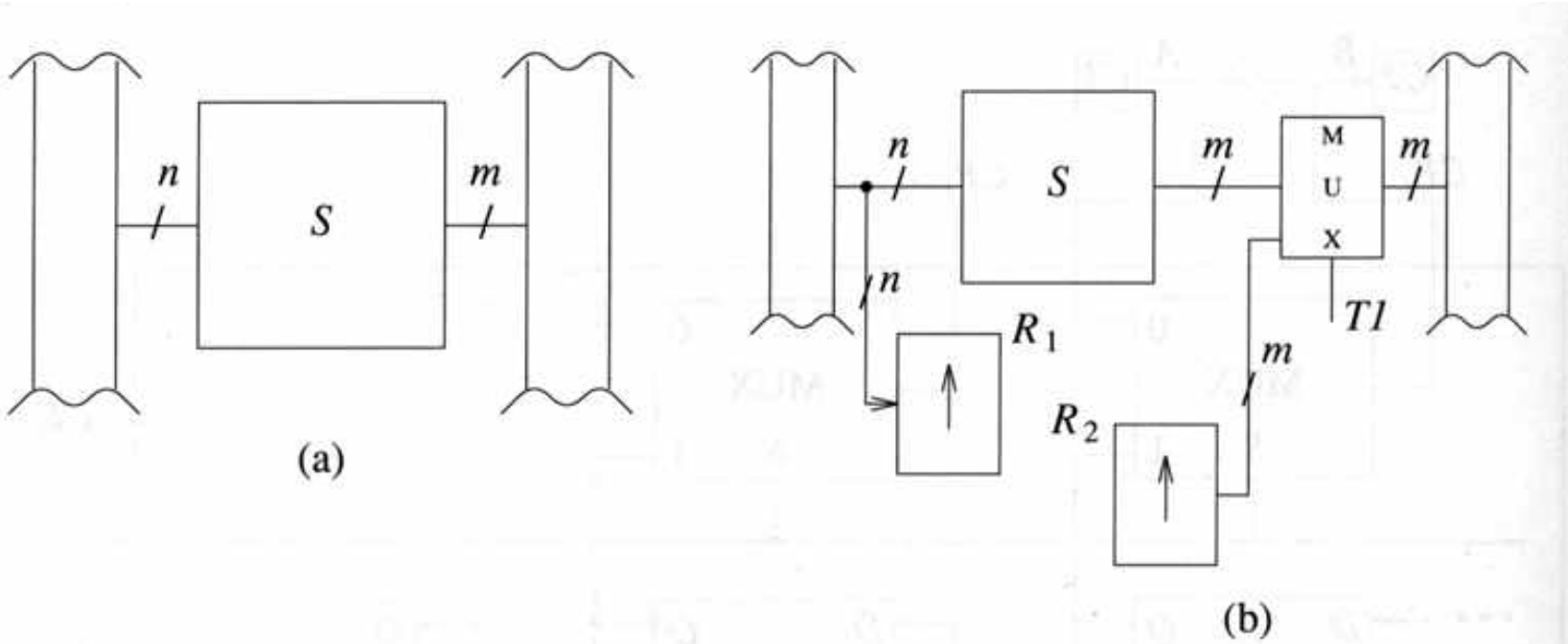


Figure 9.18 Boundary scan architecture (a) Original circuit (b) Modified circuit

System-level Boundary-scan

- Board-level testing

- Why boundary scan?
  - Efficient testing of board interconnect
  - Facilitate isolation and testing of chips

- **Standards**
  - The need for standards
  - Goal: chips contain **common DFT circuitry**
  - JTAG Boundary Scan
  - VHSIC Element-Test and Maintenance System – Bus standard
  - IEEE 1149.1 Testability Bus Standard

IEEE 1149.1

- Main elements
  - Physical structure of the test bus and how it can be interconnected to chips
  - The protocol associated with the bus
  - The on-chip test bus circuitry
    - Boundary-scan registers
    - Test access port (TAP)

The Test Bus

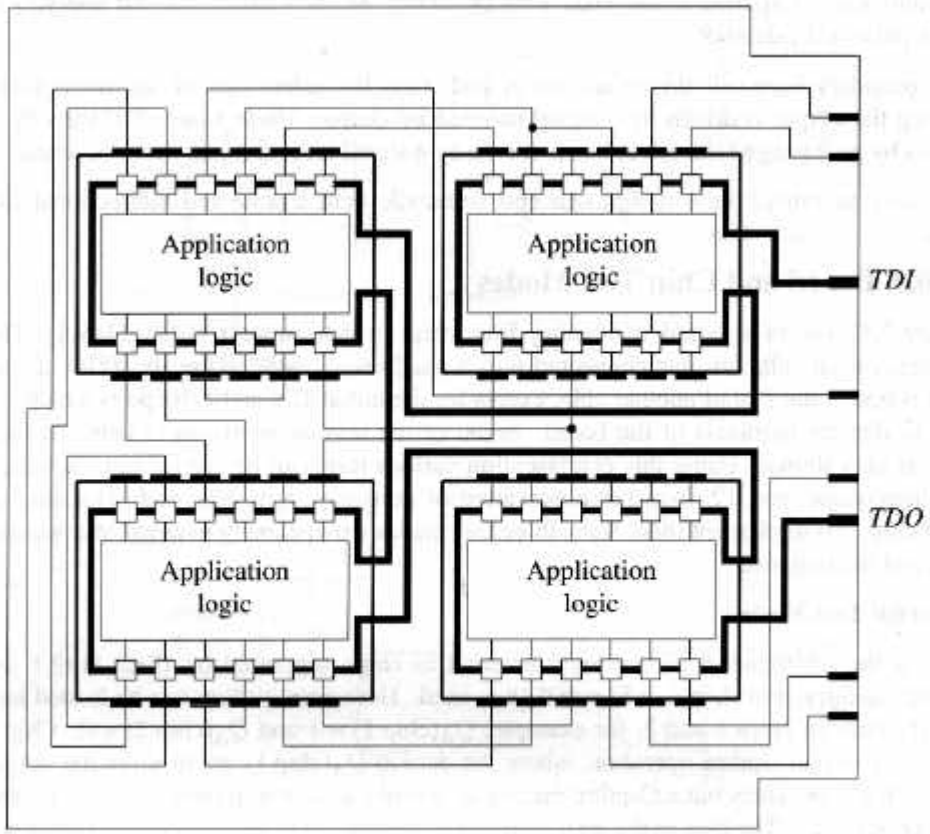


Figure 9.47 A printed circuit board with a IEEE 1149.1 test bus

- Four lines
  - Test Clock (TCK)
  - Test Data Input (TDI)
  - Test Data Output (TDO)
  - Test Mode Selector (TMS)
- Connected to chip via test access ports (TAP)
- Each chip is a bus slave

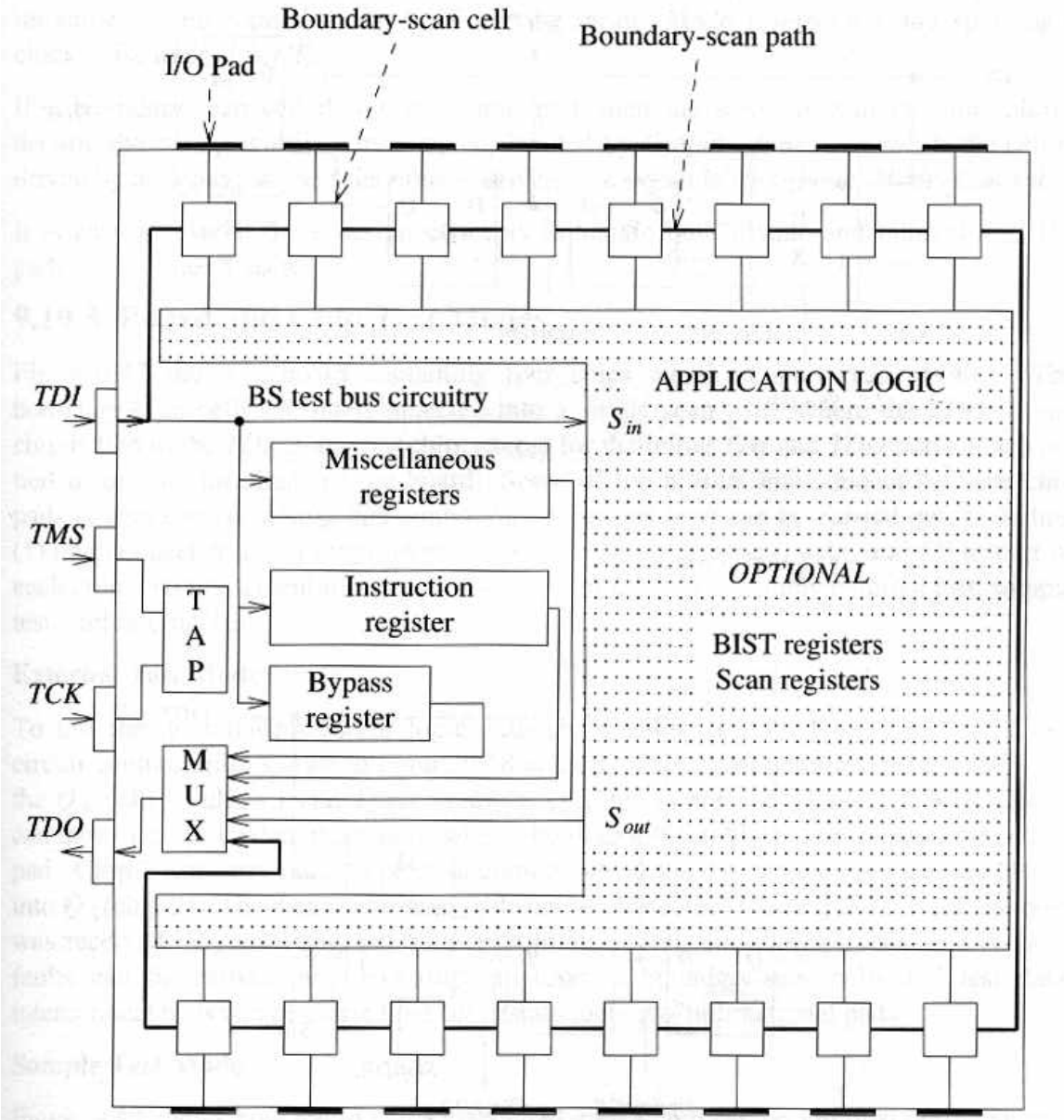


Figure 9.45 Chip architecture for IEEE 1149.1

Protocol

1. An instruction is sent serially over the TDI line into the instruction register.

2. The selected test circuitry is configured to respond to the instruction (may involve sending more data into a register selected by the instruction).

3. The test instruction is executed.
   Test results can be shifted out of selected registers and transmitted over the TDO line to the bus master.

The TAP Controller

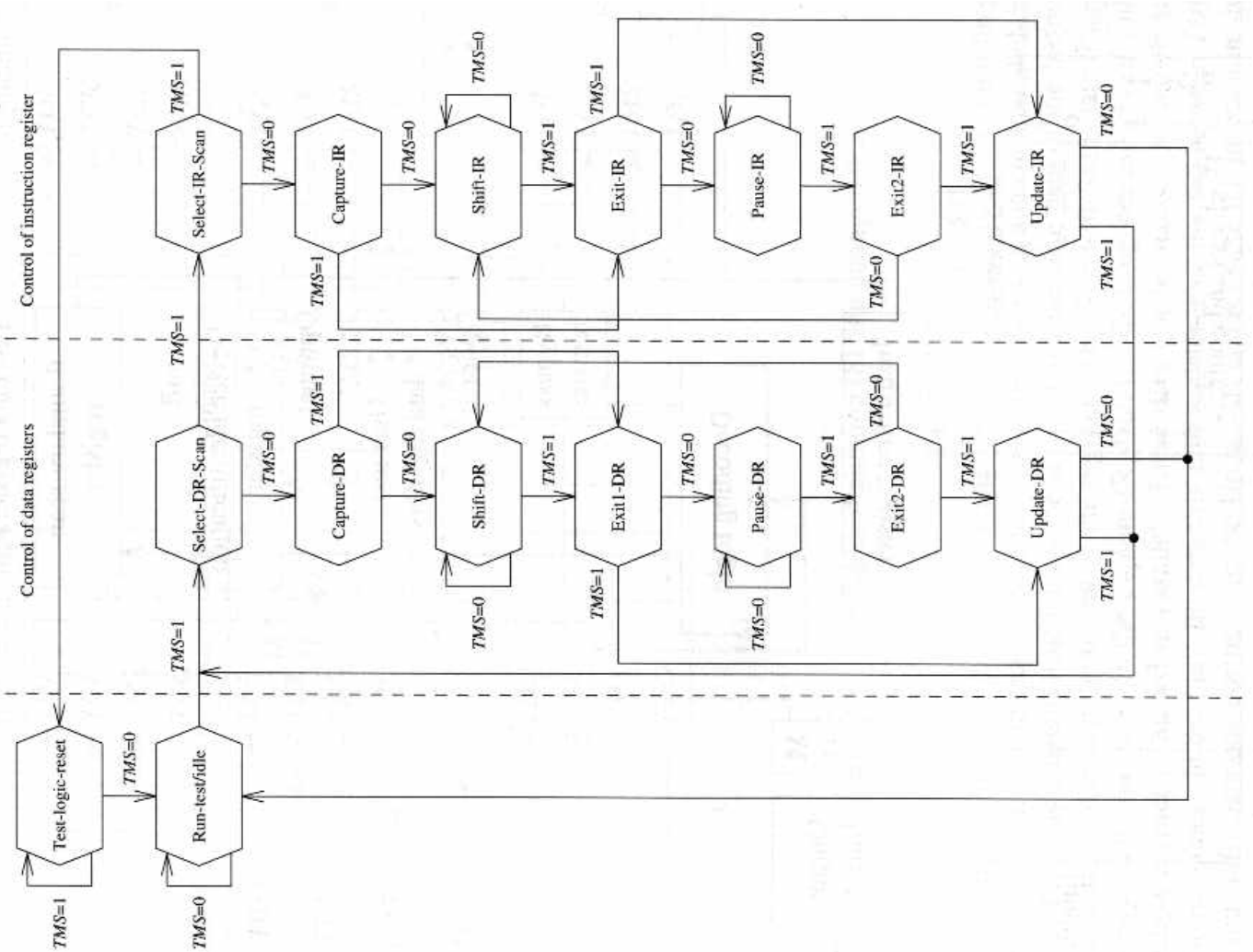


Figure 9.53 State diagram of TAP controller

Discussion

- How many **DFT methods** and techniques are there?
- How can **designers** make best use of them?
- How should the **tools** and design environments look like?
- How can we reuse the knowledge of **experience designers**?