Project Specification

OpenModelica for Mixed-Signal System Design

Description

The document outlines the specification of the 20-week project called "OpenModelica for Mixed-Signal System Design." The feasibility of using the modelica languages and the OpenModelica mainframe for IC design should be investigated. Key features are flexibility, interoperability, compatibility and low cost.

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1. INTRODUCTION

IC design becomes more and more difficult and expensive. Along with the increased cost of manufacturing IC designs, the tool costs also increases dramatically. Further on, the tools are quite conservative and do not really keep up with the pace of the industry. For example, the tool set from one of the major vendors is essentially the same it was 10 years ago. Not that much has happened, except for (smaller) incremental improvements. No major drastic changes have occurred for the design tools. It should be mentioned that the verification tools, though, improve quite a lot to be able to keep up with fabrication.

1.1 The Master's Thesis' Projects at Electronics Systems, Dep't of E.E., LiU

At the division of Electronics Systems, Department of Electrical Engineering, we are striving towards project-oriented final-year projects where many students can be supervised in a shared forum. This is a multi-voiced supervision approach. The projects are tightly related to the research at the division and the researchers will also take part in the shared forum. The students and researchers will work on a shared platform, in which the students and researchers contribute with small bits and pieces.

2. PROJECT DESCRIPTION

This project, “OpenModelica for Mixed-Signal System Design”, is about investigating the openModelica tool (and related software in the tool suite) and the modelica language to define mixed-signal circuits for IC design.

Already today there are basic building blocks for electronic design available for Modelica. These are however mainly oriented towards discrete-component design for PCB, etc. We would like to extend the packages to also cover submicron IC design building blocks. Blocks could be filters, data converters, interpolation and decimation filters, etc.

The student needs to find ways how to model these blocks and how to be able to interact with other tool vendors. Could for example OpenModelica be used for simulation, whereas the netlist defining the topology of the circuit is given by another tool. Or vice versa.

However, the Modelica languagae and the OpenModelica tool might be more suited for higher-level system design. This might imply that this project will be more oriented towards analog description languages, like verilogA, verilog-AMS, ahdl, vhdl-a, etc.
Notice that the job might also include developing your own additions to the OpenModelica framework.

The students can also interact with project EXJOBB_0023:OpenModelica for analog IC Design.

2.1 Suggested Start of the Project -- Literature Study

It is suggested that the student starts with a literature search on the internet/library to get familiar with the concepts:

- Freeware tools for IC design
- IC design tools
- Circuit design tools
- OpenModelica
- Modelica

2.2 2nd Phase -- Model Description

The next phase of the project is to start implementing the models in modelica and simulated/verify in OpenModelica. It might be required that the student also needs to sit down with conventional design tools to benchmark the two tools against each other.

The implementation of the model should take all effects into account required to demonstrate that the components can be implemented in a modern CMOS process.

2.3 3rd Phase -- Schematic-Level Description

The third phase of the project is to implement more advanced test circuits with OpenModelica to demonstrate the capabilities of the tool.

2.4 Final Phase -- Demonstrator

The final phase of the project is to implement a demonstrator including tutorial documentation. The specification of this demonstrator is still TBD, but will be defined once the student joints the project.

2.5 Example on Suitable Sources for Literature Studies

Start for example with the following pages:

http://www.openmodelica.org/
http://www.cadence.com
http://www.synopsys.com
http://www.mentor.com
Any search on the internet for buzz words like

freeware IC design tools

Within the literature study in particular

modelica and openmodelica

3. DETAILED SPECIFICATION

Table 3.1 compiles the detailed project design specification. The table is subject to change, but is added to the document for an orientation and reaction upon. All values are valid for all corner conditions.

<table>
<thead>
<tr>
<th>Item</th>
<th>Comment</th>
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<tbody>
<tr>
<td>Building blocks</td>
<td>The software should address important building blocks such as analog filters, digital filters, ADC, DAC, PLL, DLL</td>
</tr>
<tr>
<td>Parameterization</td>
<td>All the above mentioned building blocks should be possible to parameterized using physical and electrical design parameters</td>
</tr>
<tr>
<td>Schematic entry</td>
<td>There should be a way to connect these components together and move them around.</td>
</tr>
<tr>
<td>Platforms</td>
<td>The implemented software cannot be too obscure*there must be porting capabilities to other software vendors</td>
</tr>
</tbody>
</table>

Table 3.1: Project specification

3.1 Examples on Demonstrator

An example of an building block that can be used as demonstrator for the exjobb:

- a Tx/Rx chain for DSL
- a Tx/Rx chain for WCDMA
- an all-digital DLL/PLL

4. THESES PROJECTS AT ELECTRONICS SYSTEMS

This chapter outlines the students' working environment at the Electronics Systems (ES) group at the department of Electrical Engineering (ISY), Linköping University (LiU).
4.1 Working Environment

The student is initially offered a seat in one of ES’ two research laboratories. Currently there is a lack of office space for the students, and we have a queue system in which the student has to stand in line to eventually get a seat. The queue is active from 2010 and onwards.

You will get swipe card access for a 6-month period and if you are in need of a key this will be provided to you too. The key will give you access to the ES coffee room and potentially some of the offices.

Within the project we are going to use Cadence, Synopsys, and Matlab software tools. It is however strongly encouraged to also look at and use freeware tools like Electric VLSI, Magic, ngSpice, gnucap, and octave.

The student should use Openoffice or LaTeX for documentation. It is strongly encouraged that the student updates the documentation on a daily or at least weekly basis. The documentation should be made available on the shared project disk area for anyone to access and read. Especially since the different members of the exjobb group will interact with each other.

Since there will be students and researchers joining the project continuously, the junior project members should take the opportunity to discuss with senior project members about fundamentals properties of the project flow and the target system.

4.2 Communication

The ambition is to have a weekly forum where the whole EXJOBB team meets to discuss and interact. It is strongly advised that the students take the opportunity to bring questions forward. The meeting will start with a 15-minute around-the-table using the SCRUM model. The supervisor will then have a 30 to 45-minute lecture regarding for example documentation principles, design practice, programming, etc. During the second hour we focus on one of the building blocks, i.e., one of the student projects.

Further on, it is strongly encouraged to send e-mails to the group list:

digital-analog@googlegroups.com

Please send all questions to the supervisor in advance and also send to the other group members too via this address, such that we can share information and keep discussion threads alive. It is also advantageous that we are able to read through old e-mail conversations during the documentation phase.

Store as much information as possible in the shared database (even simulation results if required). such that the supervisors can access the material during out-of-office hours.

4.3 Plagiarism

The University will from 2010 introduce more quality checks on the student projects. Random samples will be picked from for example master theses and then checked by some independent group. This also means that the theses then will be checked for plagiarism and citing errors (if the citing and quotations are incorrect, it will be considered as plagiarism, i.e., cheating). This checking can be done by yourself in advance by sending the document to a special server e-mail address:
The student is encouraged to be careful when citing and quoting reports, papers and books. Browse the link below for more information.

http://people.kth.se/~ambe/KTH/Guidingstudents.pdf

There are plenty of examples on e.g. how many words you can use in a quote before it is considered to be plagiarism, etc., etc.

4.4 Letter of Intent
The student will also get a time plan to be signed by both the supervisor and the student. This time plan includes mile stones and examples on important project deliverables.

It is very important that the student takes responsibility of his own project. It is important that the anticipations of the student aligns with the anticipations of the supervisor. The time plan document should reflect this mutual understanding and be understood by both parties.

The time plan document is not a legal document.

4.5 Ambition Level
The ambition levels with the projects are supposed to be high. It would be very good to be able to write up an academic conference contribution using the outcome of the project. There are also other 'competitions' to which you can send your exjobb and compete for the title best student project of the year, etc.

Also, please indicate to the supervisor your own ambition levels and what you want to achieve with your project.

4.6 Reflection Document
After completed Master's thesis you should provide a personal reflection document. In this two-page document you should evaluate your own work. You can, if you like, comment on supervisors, etc., etc., but remember once again that you are in charge of your own work and you must take the actions if required.

4.7 Examples on Deliverables
See the time plan (EXJOB0.0024_TP) for more detailed information, but examples are document disposition, simulation models, top level specifications.