STRINGENT NEWS

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This is the first Newsletter from Stringent (Strategic Integrated Electronic Systems Research at Linköping University).

We hope you will enjoy it!

The newsletter is intended to keep in touch with you. We seek contact and cooperation with industry and institutes worldwide, in the field of electronics and electronics design. Being located close to Stockholm, we are centered in the Nordic countries, but consider ourselves European.

Stringent is a research center at Linköping University, Sweden, financed by Swedish Foundation for Strategic Research, and aimed for electronic design. We are the largest electronics research center in Sweden, with about 50 people. Stringent was created 2003 by combining the resources of four professor chairs, Electronic devices (Professor Atila Alvandpour), Computer engineering (Professor Dake Liu), Electronics systems (Professor Lars Wanhammar) and Embedded systems (Professor Zebo Peng). After two and a half years of Stringent activity, our founder evaluated us this summer with very good results.

— Christer Svensson, Professor and Stringent director

Programmable RF systems—a new vision

This first issue of the newsletter is devoted to "Programmable RF systems". We have identified this topic as a new vision for the center, aiming at making the software defined radio (SDR) possible. Other applications could be radar systems, or combined radio and radar. Our vision is to be able to build programmable hardware that can manage all kinds of RF systems from antenna to applications, at carrier frequencies of, say 1–10GHz, and without cost or power penalty. We describe some recently achieved results aiming in this direction in this issue of the newsletter. Stefan Andersson writes about flexible RF front-ends, Per Löwenborg describes our work on flexible AD converters and Eric Tell describes his Ph.D. thesis about a programmable radio base-band processor.

Excellent grades

An international committee evaluated all microelectronics research financed by Foundation for Strategic Research in Sweden this summer. The committee members were Profs. D. Bimberg, Berlin, C. Jagadish, Canberra, Q. Huang, Zürich, H. Maes, Leuven, V. Oklobzia, Davis and W. Stewart, Innos. Regarding Stringent the committee wrote: ***"This is a very strong program, one of the strongest in the group of programs reviewed. It is recommended that they keep on their excellent work."*** We are of course very happy for this, and will do our best to keep up with the expectations.

Flexible RF Front-Ends

The vision of having a generic RF front-end that can be programmed to any given standard, in the same way as microprocessors, has been a dream for a long time. The basic idea is to convert the RF signal directly to digital form and then perform all signal processing in the digital domain. The traditional view of software-defined radio (SDR), where the analog-to-digital converter (ADC) is placed directly at the antenna or after the low-noise amplifier (LNA), puts unrealistic requirements on the ADC in terms of sampling rate and resolution resulting in too high power consumption. This is the main reason why SDR is more a vision than reality today except for low carrier frequencies where SDR can be built. However, a lot of things are happening today within this area due to the enormous need for low cost multi-standard RF front-ends because of the steadily increasing number of standards used around the world.

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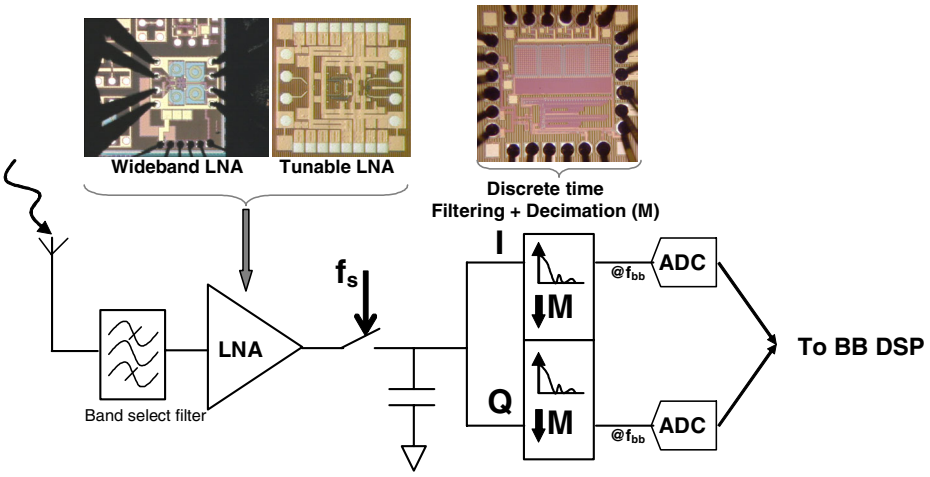

Figure 1. RF-sampling front-end

The key to success is to have an RF front-end architecture that is highly flexible (reconfigurable) without putting too tough requirements on the ADC. One approach to do this is the RF-sampling front-end in Figure 1. The basic idea is to sample the RF signal after the LNA and do further processing and necessary decimation before analog-to-digital conversion. Today's CMOS technologies demonstrate very high speeds, making the RF sampling technique appealing in a context of multi-standard operation at GHz frequencies.

This flexible RF-front-end also requires a flexible multistandard LNA. Two approaches to this have been investigated and designed. The first topology was a wideband LNA covering all the frequency bands of interest (up to 6 GHz) while the second was a widely tunable LNA (measured tuning range 0.75–3 GHz, measured noise figure 5 dB) based on the principle of active recursive filters.

Looking at the RF front-end, the traditional mixer is replaced by a sampler (zero-IF conversion) and a discrete-time switched capacitor (SC) filter, which renders the design to be more robust and more flexible in frequency planning. At the same time decimation is performed to decrease the sample rate from a value close to the carrier frequency to a value suitable for analog-to-digital conversion. A high sample rate is still wanted to utilize oversampling in the ADC.

An experimental chip successfully demonstrated the reception of 54 Mb/s data rate utilizing 64-QAM modulation of a 2.4 GHz carrier frequency. The high I/Q accuracy needed for 64-QAM modulation was easily obtained by using the same LO phase for both I and Q sampling (see figure). We further demonstrated that the same hardware can be used for various carrier frequencies by just changing the LO frequency.

— *Stefan Andersson, Ph.D. student*

Flexible AD Converters Enable SDR

The evolution of digital signal processing (DSP) has enabled the fast growth of mobile communication systems and has led to new sophisticated medical aids (just to mention a couple of important applications). The foremost advantages of DSP over its counterpart, analog signal processing (ASP), are its robustness and that it can perform functions with arbitrary precision. Our world is, however, analog by nature which means that the need for analog signal processing cannot be eliminated completely. In particular, it will always be necessary to use *analog-to-digital converters* (ADCs) in order to convert analog quantities such as sensor data and electromagnetic waves into digital representations for further processing.

In all A/D-converter architectures and technologies known today, it is very difficult to simultaneously achieve high resolution and high sampling rate. Such speed/resolution trade-off is very common in analog circuit design. Resolution is to a large extent determined by matching accuracy of physical devices. For example, in MOS technology, the variance of the matching error of two devices is a function of the inverse of the area of the devices. Hence, when increasing the

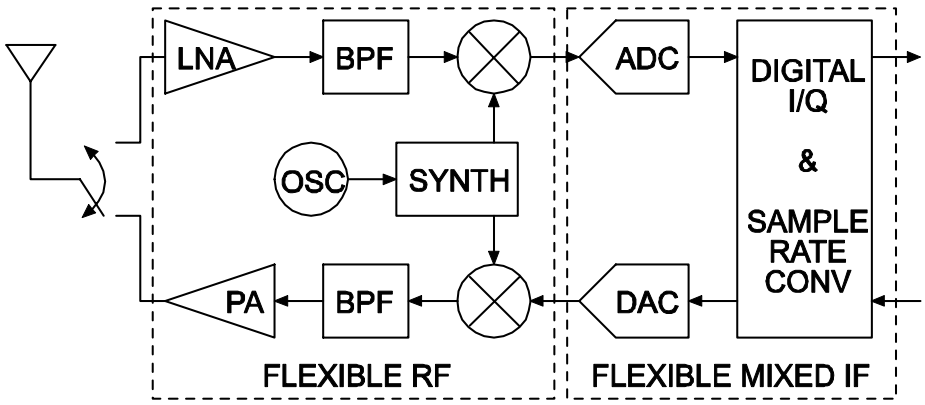

Figure 2. Digital-IF transceiver with flexible RF and mixed-signal

area the matching will be improved and the accuracy is increased. However, increasing the area also increases the parasitic capacitance of the devices which in general decreases the operational bandwidth of the circuit and thereby reduces the speed. A third, very important parameter is power consumption.

In addition to the traditional resolution and sampling rate requirements, new objectives are arising in terms of *flexibility* and *multi-mode operation* which are driven by current academic and industrial interests in software defined radio and radars. The most promising approach to achieve high- performance, multi-mode, and flexible operation is to combine software-defined functionality with flexible circuits, in particular *flexible RF frontends and flexible data converters*. This means that both the RF front-ends and data converters must be able to handle adjustable bandwidths, centre frequencies, and dynamic range. One possible transceiver architecture for software-defined radio, containing both flexible RF and mixed-signal parts, is shown in Figure 2.

The major reasons for using flexible RF front-ends and data converters are energy efficiency, multi-mode operation, and the possibility to achieve reprogrammability. The energy efficiency is achieved by optimizing the performance to what is actually required for each operation mode, while multi-mode operation on a single platform substantially reduces the overall hardware cost. Flexibility increases the design efficiency and extends the operating lifetime of the system and is therefore a major cost saver.

An interesting set of candidate architectures for flexible A/D conversion is delta-sigma (ΔΣ) modulators. These have received a great attention during the past decades mostly due to their possibility to realize high-resolution analog-to-digital conversion without the need for high-precision analog components. The foremost property of ΔΣ-modulators that makes them suitable for flexible operation is their inherent bandwidth/resolution trade-off. That is, the oversampling ratio M can be used directly to trade analog bandwidth for resolution. This is true both for lowpass and bandpass ΔΣ-modulators. Other means to achieve flexibility, particularly useful for bandpass ΔΣ-modulation, are flexible sample frequency and programmable loop filters.

— *Per Löwenborg,*
Assistant Professor

A programmable baseband processor

The integration of more and more functions in small handheld radio terminals makes it interesting to use a programmable baseband processor for the heavy digital signal processing necessary in modern radio standards. That way the same modem hardware can be reused between different standards instead of using separate fixed function blocks for each standard (such as 3G, GSM and Bluetooth), which is what people usually do today.

The new architecture was successfully implemented as a prototype chip in 0.18μm CMOS. This chip runs WLAN standards 802.11a and b at a power consumption of 80 mW utilizing a silicon area of 2.9 mm^2, including memories. It is therefore more efficient than a single standard ASIC!

In addition to saving silicon area, a programmable baseband processor may also lead to reduced development times, since the same hardware can be used in different products and only new software has to be developed. Furthermore, product lifetime can be improved since software patches can be downloaded to support new standards and functions.

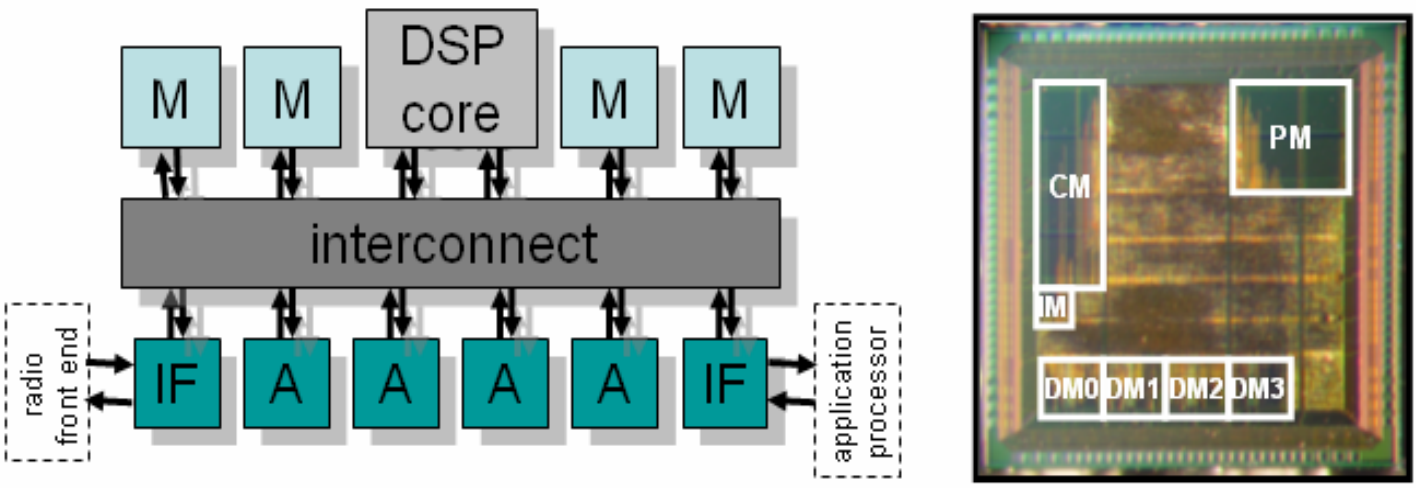

Figure 3. Programmable baseband processor architecture and prototype chip

The Ph.D. thesis "Design of Programmable Baseband Processors" focuses on the design of multi-standard baseband processors, mainly aimed at battery powered devices where low cost and power consumption is essential.

The work describes a novel architecture (see Figure 3) and assembly instruction set optimized for radio baseband processing, as well as selection, integration, and design of hardware accelerators for jobs that are not suitable for software implementation.

— *Eric Tell, Ph.D.*

Final projects at Philips

Many students from Stringent are doing their final project at Philips, Eindhoven. Such cooperation helps to strengthen the contacts between Philips and Stringent, and may lead to further research contacts. We can report six recent examples.

Daniel Boijort and Oscar Svanell, "Pulse width modulation for on-chip interconnects", Joel Hedestig, "Design of a MEMS-resonator time-base oscillator system" and Jayanth Kalyan, "Low power SDR/DDR SDRAM I/O power modeling" were completed with Dr. Atul Katoch, Dr. Cicero Vaucher and Dr. Jan Vink as industrial supervisors respectively, and with Prof. Atila Alvandpour as examiner.

Urban Ingelsson, wrote his thesis "Test Scheduling for modular SoCs in an abort-on-fail environment" under supervision of Erik Jan Marinissen and Sandeep Goel Kumar with Erik Larsson as examiner.

Xiao Ru, wrote his thesis "Synchronous latency insensitive design in the Æthereal NoC" under supervision of John Dielissen and with Christer Svensson as examiner. Mr. Ru's report was then rewritten into a conference contribution and sent to ASYNC 06 in Grenoble.

Finally Tobias Dubois is presently working on his thesis with Paul Wielage, Mohamed Azimane, Erik Jan Marinissen and Clemens Wouters, and with Erik Larsson as examiner, with the preliminary title "Design and test validation of FIFO ripple buffers".

New doctors for hire!

Stringent educates new doctors continuously. In the next few months we plan two dissertations. In December 2005 Sorin Manolache defend his thesis "Analysis and Optimisation of Real-Time Systems with Stochastic Behaviour", under supervision of Professor Petru Eles, and in January 2006 Peter Caputa plans to defend his thesis "Efficient High-Speed On-Chip Global Interconnects", work which was done under the supervision of Professor Christer Svensson.

International visibility

The two most prestigious conferences in our field are International symposium on Solid State Circuits (ISSCC, every February) and Design Automation conference (DAC, every June).

In this year's DAC we had two contributions: "Fault and energy-aware communication mapping with guaranteed latency for applications implemented on NoC" by S. Manolache, P. Eles and Z. Peng, and "Quasi-static assignment of voltages and optional cycles for maximizing rewards in real-time systems with energy constraints" by A. Cortes, P. Eles, and Z. Peng.

Regarding ISSCC we have one contribution next February, "An On-Chip Delay- and Skew-Insensitive Multi-Cycle Communication Scheme" by P. Caputa and C. Svensson.

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