Activity report on STRINGENT Research Center for 2005.

Christer Svensson, Director

1. General.

STRINGENT, Strategic Integrated Electronic Systems Research, was formed January 1st 2003 by joining 4 different groups (professor chairs) at Linköping University into a common research center. The four groups are Electronic Devices, Computer Engineering and Electronic Systems at Dept. of Electrical Engineering and Embedded Systems at Dept. of Computer Science.

1.1 Program description.

STRINGENT research program has formulated the vision:

*To make Circuit and System Sciences **lead** the development of future electronics.*

This vision will be accomplished by following goals:

New methods to convert complex ideas into silicon (*System Design)*
Improve efficiency of embedded systems (*Technology utilization*)
Reduce development times (*Design efficiency*)

The main goal during 2005 was to consolidate the research center, continue to build industrial cooperation and to participate in SSF half-time evaluation. As the overall goal is to create a strong research center, we consider the SSF support for STRINGENT as a base funding for the center, on top of which there are also other funding. We consider all activities in the center as its results and do not distinguish between results obtained through different funding (except when directly asked for by SSF). During 2005 our steering committee has met 3 times and our advisory board once. We prepared a half-time report in June, which was presented for SSF evaluation committee and received very well. The center is organized into 8 project groups across the original groups and departments, lead by 8 project group leaders. We are able to report a very successful third year of STRINGENT, with for example 8 dissertations, 6 licentiates, 15 journal papers and 102 conference papers.

1.2 Project list.

The research program is organized in 8 project groups, lead by 8 project leaders. Each group is related to one of our overall goals, *System Design*, *Technology Utilization* and *Design Efficiency*. Ek, Da, Es and Em relates to the original research groups (professor chairs), Electronic devices, Computer Engineering, Electronic systems and Embedded systems. The structure has been slightly updated during 2005.

System design
Networks-on-chip (Christer Svensson)
Da1 SOCBUS
Em1 Optimization of real-time applications implemented on power constrained network-on-chip architectures
Em8 Heterogeneous networked embedded systems
Ek4 Global on-chip communication
Heterogeneous multiprocessor systems (Dake Liu)
Da2 Intra packet network processor
Da3 High end flexible DSP processor for future multimedia trans-coding
Da5 Low power base-band processor for SDR (Soft Defined Radio)
Em6 Design of heterogeneous multiprocessor systems for real-time applications
Signal processing algorithms (Lars Wanhammar)
Es4 Integrated active filters
Es5 Design and Implementation of Energy Efficient Digital Filters
Es6 Design and Implementation of Asymmetric Digital and Analog Filter Banks
Es7 Energy-efficient synchronization and equalization algorithms for multi-carrier systems
Es8 Low Power Algorithm Design and Implementation

Technology utilization

High speed interfaces (Jerzy Dabrowski)
Ek2 High speed off-chip communication
Ek5 Wide-band or tuneable low noise amplifiers
Ek11 Flexible RF frontends

AD and DA converters (Mark Vesterbacka)
Es2 Algorithms and circuit techniques for increased performance of data Converters
Es3 High performance ADCs implemented in SOI technology

High performance, low power circuit techniques (Atila Alvandpour)
Ek7 Low Power Multi-GHz Clocking
Ek8 Embedded memories
Ek9 System-on-chip synchronisation and communication techniques
Ek10 Low power, high performance processor building blocks

Efficient design

Verification (Petru Eles)
Ek3 Accurate models of AD-converters aimed for simulation
Em4 Formal verification of embedded systems in a reuse methodology
Em2 Modelling and verification of embedded systems

Testing (Zebo Peng)
Ek6 Testability-oriented design techniques for mixed-signal/RF integrated circuits
Em3 Hybrid BIST methodology for complex electronic systems
Em5 Testing system-on-chips using functional bus
Em7 Built-in self-test for ASICs and SoCs
Em9 SoC wrapper design, TAM configuration and test scheduling
Em10 Analysis and design of fault-tolerant heterogeneous embedded systems

1.3 Half-time evaluation.

The program was evaluated by SSF utilizing an international group of researchers in August 2005. The outcome for Stringent was very good: “This is a very strong program, one of the strongest in the group of programs reviewed. It is recommended that they keep on their excellent work”.

2 Graduate education.

2.1 Graduate students

29 graduate students participate in STRINGENT, of which 17 are funded by the STRINGENT program (with an average funding of 62%). For a full list of students, see below. For a list of students financed through SSF, see form 3.

Naveed Ahsan
Stefan Andersson
Alexandru Andrei
Erik Backenius
Anton Blad
Peter Caputa
Anders Ehliar
Johan Eilert
Henrik Fredriksson
Martin Hansson
Zhiyham He
Emil Hjalmarsson
Robert Hägglund
Kenny Johansson
Per Kalmström
Daniel Karlsson
Anders Larsson
Weidong Li
Behzad Mesgarzadeh
Sreedhar Natarajan
Anders Nilsson
Mattias Olsson
Traian Pop
Rashad Ramzan
Francisco Rivas
Linnea Rosenbaum
Erik Säll
Sriram Vangal
Di Wu

2.2 Graduate courses

7 Ph.D. courses was given during 2005.

Heuristic algorithms for combinatorial optimization problems, part II (Zebo Peng)

Hardware/software codesign of embedded systems (Zebo Peng)

Distributed systems (Petru Eles)

Special topics in system level design: Networks on chip (Zebo Peng, Petru Eles)

Digital signal processing (Lars Wanhammar, Håkan Johansson, Oscar Gustafsson, Per Löwenborg)

Computer arithmetic algorithms (Oscar Gustafsson)

Introduction to RF front-end design (Jerzy Dabrowski)

2.3 Theses.

During 2005 we produced 8 doctors and 6 licentiates, see below.

Ola Andersson, "Modeling and implementation of current-steering digital-to-analog converters", Ph.D., May 2005.

Henrik Ohlsson, "Studies on design and implementation of low-complexity digital filters", Ph.D, May 2005.

Magnus Karlsson, "Implementation of digit-serial filters", Ph.D, June 2005.

Luis Alejandro Cortés, "Verification and scheduling techniques for real-time embedded systems", Ph.D, March 2005.

Gert Jervan, "Hybrid built-in self-test and test generation techniques for digital systems", Ph.D, May 2005.

Sorin Manolache, "Analysis and optimization of real-time systems with stochastic behavior", Ph.D, Dec. 2005.

Eric Tell, "Design of programmable baseband processors", Ph.D, Sept. 2005.

Daniel Wiklund, "Development and performance evaluation of networks on chip", Ph.D, April 2005.

J. Carlsson, "Studies on Asynchronous communication ports for GALS systems", Licentiate, June 2005.

E. Backenius, "On reduction of substrate noise in mixed-signal circuits", Licentiate, June 2005.

E. Säll, "Implementation of flash analog-to-digital converters in silicon-on-insulator technology", Licentiate, Dec. 2005.

A. R. Mohamed, "High-level techniques for built-in self-test resources optimization", Licentiate, April 2005.

A. Larsson, "System-on-chip test scheduling and test infrastructure design", Licentiate, Nov. 2005.

L. Lindgren, "Topics on CMOS image sensors", Licentiate, Aug. 2005.

2.4. Present positions of graduated students.

Gert Jervan, Ph.D., Tallin Technical University, Estonia.
Daniel Wiklund, Ph.D., Sectra AB, Linköping.
Eric Tell, Ph.D., Coresonic AB, Linköping.
Ola Andersson, Ph.D., Ström och Gulliksson patentbyrå, Lund.
Henrik Ohlsson, Ph.D., Ericsson AB, Lund.
Magnus Karlsson, Högskolan Kalmar, Kalmar.
Luis Alejandro Cortes, Ph.D., Volvo trucks, Göteborg.
Abdil Rashic Mohamed, Licentiate, University of Dar el Salam, Tanzania.

3. Research

3.1. Participating researchers.

18 persons except students are engaged in STRINGENT, of whom 10 are partly funded by the program (with an average funding of 20%, see form 4). Participating researchers are:

Prof. Atila Alvandpour
Docent Jerzy Dabrowski
Dr. Anders Edman
Prof. Petru Eles
Prof. Håkan Johansson
Dr. Erik Larsson
Prof. Dake Liu
Dr. Per Löwenborg
Dr Aziz Ouacha
Dr Kent Palmkvist
Prof. Zebo Peng
Dr. Paul Pop
Prof. Christer Svensson
Dr. Ingemar Söderquist
Prof. Mark Vesterbacka
Prof. Lars Wanhammar

3.2 Publications.

The Research activity during 2005 has resulted in 15 papers in scientific journals, 6 book chapters, and 102 papers in scientific conferences, of which 1 were invited. 9 silicon chips has been taped out and 9 have been evaluated. 4 patents or patent applications were reported. For a publication list, see Appendix 1.

3.3 Workshops

Stringent initiated a series of internal workshops during 2005. The first workshop, "Signal processing for communication" occurred on Nov. 7.

4. External activities.

4.1 Cooperation with Swedish industry.

We have performed some design work for Sicon Semiconductor AB.
One of our researchers (C. Svensson) is a board member of Switchcore AB (publ.) and Coresonic AB.
A new network has been formed, Lincom (Linköping Communication), on the initiative of local industry, Saab, Ericsson and Sectra. Lars Wanhammar represents Stringent.

4.2 Spinoff companies.

We have had close cooperation with the two new companies formed from STRINGENT during 2004, *Signal processing devices Sweden AB* and *CoresonicAB.*

4.3 Cooperation with foreign industry.

We have 4 research grants from foreign industry, 50kUSD and 40kUSD from Intel (USA), and 75kUSD from Intel (USA), Infineon (Germany) and Samsung (Korea). We have further received 400kRMB (¨50kUSD) from ICC Shanghai, China, to be used for a Ph.D. student from ICC Shanghai.

4.4 Additional research funding.

Several research applications were prepared during 2005, of which 3 were granted:
3 project applications at Vetenskapsrådet were granted, totally 2494ksek/yr in 3 years.
A joint research project with FOI, "Cognitive microwave electronics" was initiated.

4.5 Cooperation with other Swedish programs.

A national conference, SSoCC was arranged April 18-19 in Tammsvik in cooperation with Socware and FlexSoC.

A national summer school, Intelect, was arranged in Visby in cooperation with Ramsis, KTH, August 29-31, 2005. A book is planned to be edited on the course material.

Together with IFM, LiU, we arranged SSF Program Conference on Microelectronics, Aug. 24-15 in Linköping.

We arranged a workshop on Wireless systems together with Ramsis, KTH, in Linköping on March 23.

4.6 Webpage

The webpage is found at http://www.ida.liu.se/~eslab/stringent/. Responsible person is Alexandru Andrei.

4.7 Information about the program.

In fall 2005 Stringent published a first Stringent Newsletter, which was sent out to all Stringent members and to all Stringent industrial and other contacts. The newsletter was well received and several feedbacks have been noted (It was even cited in a keynote speech at a large international conference). The intention is to publish the Newsletter twice a year, on different themes.

Stringent has been presented at a number of occasions. For example for the Swedich EDA group and for the Swedish national network for DFT research. It has also been presented to Sony-Ericsson, IAR, Volvo, Intel (Portland) and Micron (Boise).

We note quite some publicity related to our digital baseband research and the Coresonic spinoff 2004: University news: "Stringent spinoff…", Ny Teknik: "Mobiluppfinning basen i nytt Linköping…", KISTA Science city: "Ny processor stödjer alla mobila nät", TV4 Öst morning news, Elektroniktidningen "Linköping knoppar av basbandskrets", and SIS Research news: "Software-defined radio simplifies mobile phones".

5. Program administration.

The program has been managed by the program director, prof. Christer Svensson, with support from assistant Anna Folkesson

5.1 Steering committee.

The Steering committee has met 3 times during 2005. The members are:
Magnus Danestig, Flextronics, chairman (magnus.danestig@se.flextronics.com)
Jan Grahn, CTH (jan.grahn@mc2.chalmers.se)
Jonas Plantin, Ericsson (jonas.plantin@ericsson.com)
Mikael Rudberg, Infineon (mikael.rudberg@infineon.com)
Lars Svensson, CTH (larssv@ce.chalmers.se)

5.2 Advisory board.

The Advisory board met in mars 2005. The members are:

Shekhar Borkar, Intel, USA (Shekhar.y.borkar@intel.com)
Manfred Glesner, T U Darmstadt, Germany (glesner@mes.tu-darmstadt.de)
Gunnar Björklund, Infineon, Sweden (gunnar.bjorklund@infineon.com)
Christain Piguet, CSEM, Switzerland (christian.piguet@csem.ch)
Tor Ramstad, NTNU, Norway (tor@tele.ntnu.no)

5.3 Monthly letter.

In order to keep all participants in Stringent aware of various events and news, the director writes a monthly letter (since August 2004) which is distributed to everyone and posted at the website.

Linköping, March 6, 2005,

Magnus Danestig Christer Svensson
Chairman Director

STRINGENT 2005, Appendix 1, Publications.

Books and book chapters

1. G. Jervan, R. Ubar, Z. Peng and P. Eles, "Test Generation: A Hierarchical Approach," Chapter in System-Level Test and Validation of Hardware/Software Systems, Springer Series in Advanced Microelectronics, Vol. 17, ISBN 1-85233-899-7, 2005, pp. 67-81.

2. G. Jervan, R. Ubar, Z. Peng and P. Eles, "An Approach to System-Level DFT," Chapter in System-Level Test and Validation of Hardware/Software Systems, Springer Series in Advanced Microelectronics, Vol. 17, ISBN 1-85233-899-7, 2005, pp. 121-149.

3. E. Larsson, "Introduction to Advanced System-on-Chip Test Design and Optimization," FRONTIERS IN ELECTRONIC TESTING : Volume 29,, Springer, ISBN: 1-4020-3207-2, May 2005.

4. Dake Liu and Eric Tell, “Low power Baseband Processors for Communications”, Chapter 23 in Low Power Electronics Design, Edited by professor Christian Piguet, CRC Press, ISBN 0-8493-1941-2, 2005

5. P. Pop, P. Eles and Z. Peng, “Distributed Embedded Real-Time Systems: Analysis and Exploration”, Chapter in Embedded Systems Design: The ARTIST Roadmap for Research and Development, Lecture notes in Computer Science, Vol. 3436, ISBN 3-540-25107-3, 2005.

6. P. Pop, R. Ernst, P. Eles and Z. Peng, “Automotive Industry”, Chapter in Embedded Systems Design: The ARTIST Roadmap for Research and Development, Lecture notes in Computer Science, Vol. 3436, ISBN 3-540-25107-3, 2005.

Journal papers

1. S Andersson and C Svensson, “An Active Recursive RF Filter in 0,35 um BiCMOS”. In Journal of Analog Integrated Circuits and Signal Processing, Vol 44, No. 3, September 2005, pp 213-218.

2. S Andersson and C Svensson, “Direct experimental verification of shot noise in short channel MOS transistors”. In IEE Electronics Letters, Vol 41, No. 15, July 2005, pp 869-871.

3. S Andersson, J Konopacki, J Dabrowski and C Svensson, “SC Filter for RF Sampling and Downconversion with Wideband Image Rejection”, accepted to Int. Journal on Analog Integr. Circuits and Signal Processing, Kluwer-Springer.

4. K.O. Andersson and M. Vesterbacka, "Modeling of glitches due to rise/fall asymmetry in current-steering digital-to-analog converters," accepted for publication in *IEEE Trans. Circuits Syst.*, I, Vol. 52, No. 11, pp. 2265-2275, Nov. 2005.

5. A. Andrei, M. Schmitz, P. Eles, Z. Peng and B. M. Al-Hashimi, “Overhead-Conscious Voltage Selection for Dynamic and Leakage Energy Reduction of Time-Constrained Systems”, IEE Proceedings Computers & Digital Techniques, special issue with the best contributions from the DATE 2004, Vol 152, pp. 28-38, January 2005.

6. P. Caputa and C. Svensson, ”Well-Behaved Global On-Chip Interconnect ”.In IEEE Transactions on Circuits and Systems, Vol 52, No 2, February 2005, pp 318-323.

7. D. Jakonis, K. Folkesson, J. Dabrowski, P. Eriksson and C. Svensson, “A 2.4-GHz RF Sampling Receiver Front-End in 0.18-µm CMOS”. In IEEE Journal of Solid-Stated Circuits, Vol 40, No 6, June 2005, pp 1265-1277.

8. H. Johansson and O. Gustafsson, "Linear-phase FIR interpolation, decimation, and Mth-band filters utilizing the Farrow structure," *IEEE Trans. Circuits Syst*. I, vol. 52, no. 10, pp. 2197-2207, Oct. 2005.

9. E. Larsson, J. Pouget and Z. Peng, "Abort-on-Fail Based Test Scheduling," Journal of Electronic Testing; Theory and Applications (JETTA), Vol. 21, No. 6, Dec. 2005, pp. 651-658.

10. L. Lindgren, J. Melander, R. Johansson and B. Möller, “A Multi-resolution 100-GOPS 4-Gpixels/s Programmable Smart Vision Sensor for Multi-sense Imaging”. In IEEE Journal of Solid-State Circuits, Vol 40, No 6, June 2005, pp 1350-1359.

11. R. Mohamed, Z. Peng and P. Eles, "A Wiring-Aware Approach to Minimizing Built-In Self-Test Overhead," Journal of Computer Science and Technology, Vol. 20, No. 2, March 2005, pp. 216-223.

12. Z. Peng, E. Larsson and P. Eles, "Editorial: Emerging Strategies for Resource Constrained Testing of System Chips," IEE Proceedings Computers & Digital Techniques, Special issue, Vol. 152, No. 1, Jan. 2005, pp. 65-66.

13. J. Pouget, E. Larsson and Z. Peng, "Multiple Constraints Driven System-on-Chip Test Time Optimization," Journal of Electronic Testing; Theory and Applications (JETTA), Vol. 21, No. 6, Dec. 2005, pp. 599-611.

14. R. Ramzan, J. Dabrowski, "CMOS Blocks for on-Chip RF Test", accepted to Int. J. Analog Integrated Circuits and Signal Processing, Kluwer-Springer.

15. M. Varea, B. M. Al-Hashimi, L. A. Cortes, P. Eles, Z. Peng, "Dual Flow Nets: Modeling the Control/Data-Flow Relation in Embedded Systems", ACM Transactions on Embedded Computing Systems (accepted for publication).

Conference papers

1. A. Andrei, M. Schmitz, P. Eles, Z. Peng and B. M. Al-Hashimi, “Quasi-Static Voltage Scaling for Energy Minimization with Time Constraints”, Design Automation and Test in Europé Conference (DATE2005), pp. 514-519, March 2005.

2. S. Andersson and C. Svensson, “A 750MHz to 3GHz tunable narrowband low-noise amplifier. In proceedings of the 23rd Norchip conference, Oulu, Finland, Nov 21-22, 2005, pp 8-11.

3. S. Andersson, J. Konopacki, J. Dabrowski and C. Svensson, “ RF-sampling mixer for zero-IF receiver with high image-rejection”, MIXDES 2005, Krakow Poland, June 22-24, 2005, pp.185-188

4. S. Andersson and C. Svensson, “A widely tunable narrowband low-noise amplifier”, Radio Science and Communication conference, RVK, Linköping, June 14-16 2005, pp 501-504.

5. S. Andersson, J. Konopacki, J. Dabrowski and C. Svensson, “RF-sampling mixer for zero-IF receiver with high image-rejection”. Swedish System-on-Chip Conference, 4 p., Tammsvik, April 18-19, 2005.

6. K.O. Andersson and M. Vesterbacka, "A parameterized cell-based design approach for digital-to-analog converters," accepted for publication in Annals for Micro and Nano Systems: Special Issue for the IWSOC 2004 Conference.

7. K.O. Andersson and M. Vesterbacka, "A yield-enhancement strategy for binary-weighted DACs," accepted for publication at the European Conference on Circuit Theory and Design Cork, Ireland, Aug. 29 - Sept. 1, 2005.

8. E. Backenius and M. Vesterbacka, “Pin Assignment for Low Simultaneous Switching Noise,” Proc. Swedish System-on-Chip Conf., SSoCC’05, Tammsvik, Sweden, Apr. 18-19, 2005.

9. E. Backenius and M. Vesterbacka, “Introduction to Substrate Noise in SOI CMOS Integrated Circuits,” Proc. National Conf. on Radio Science, RVK’05, Linköping, Sweden, June 14-16, 2005.

10. E. Backenius, E. Säll, and O. Gustafsson, "Bidirectional Conversion to Minimum Signed-Digit Representation," to appear in Proc. IEEE Int. Symp. Circuits Syst., Kos Island, Greece, May 21-24, 2006.

11. A. Blad, O. Gustafsson, and L. Wanhammar, "Implementation aspects of an early decision decoder for LDPC codes," Proc. IEEE NorChip Conf, Oulu, Finland, Nov. 21-22, 2005.

12. A. Blad, O. Gustafsson, and L. Wanhammar, "A hybrid early decision-probability propagation decoding algorithm for low-density partiy-check codes," Asilomar Conf. Signals, Syst., Comp., Pacific Grove, CA, Oct. 30-Nov. 2, 2005.

13. A. Blad, O. Gustafsson, and L. Wanhammar, "An early decision decoding algorithm for LDPC codes using dynamic thresholds," European Conf. Circuit Theory Design, Cork, Ireland, Aug. 29-Sept. 1, 2005

14. A. Blad, O. Gustafsson, and L. Wanhammar, "An LDPC decoding algorithm utilizing early decisions," National Conf. Radio Science (RVK), Linköping, Sweden, June 14-16, 2005.

15. A. Blad, O. Gustafsson, and L. Wanhammar, "Early decision decoding methods for low-density parity-check codes," in Proc. Swedish System-on-Chip Conf., Tammsvik, Sweden, April 18-19, 2005.

16. D. Bäckström, G. Carlsson and E. Larsson, “Boundary-Scan Test Control in the ATCA Standard”, IEEE European Board Test Workshop (EBTW), Tallinn, Estonia, May 25-26, 2005.

17. P. Caputa and C. Svensson, “A 3Gb/s/wire, 5mm Long, Low Latency, Global On-Chip Bus in 0.18µm CMOS”. Swedish System-on-Chip Conference, 2 p., Tammsvik April 18-19, 2005.

18. P. Caputa, R. Källsten and C. Svensson, “Capacitive crosstalk effects on on-chip interconnect latencies and data-rates”, In proceddings of the 23rd Norchip conference, Oulu, Finland, Nov 21-22, 2005, pp 281-284.

19. J. Carlsson, K. Palmkvist, and L. Wanhammar, "GALS port implementation in FPGA", National Conf. Radio Science (RVK), Linköping, Sweden, June 14-15, 2005.

20. L. A. Cortes, P. Eles, Z. Peng, "Quasi-Static Scheduling for Multiprocessor Real-Time Systems with Hard and Soft Tasks", 11th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA'05), Hong Kong, August 17-19, pp. 422-428

21. L. A. Cortes, P. Eles, Z. Peng,, "Quasi-Static Assignment of Voltages and Optional Cycles for Maximizing Rewards in Real-Time Systems with Energy Constraints", 42nd Design Automation Conference, Anaheim, CA, June 13-17, 2005, pp. 889-894

22. J. Dabrowski and J. Gonzalez Bayon, “Techniques for Sensitizing RF Path under SER Test”, ISCAS, Kobe, Japan, May 23-26, 2005, pp 4843-4846.

23. A. Edman, C. Svensson and B. Mesgarzadeh, “Synchronous Latency-Intensive Design for Multiple Clock Domain”, IEEE Int. Soc Conference (SoCC), 25-28 Sept 2005, Washington, USA.

24. A. Ehliar and D. Liu, “Flexible route lookup using range search”, Proc of the The Third IASTED International Conference on Communications and Computer Networks (CCN), Marina del Rey, CA, USA, Oct 2005

25. A. Ehliar, D. Wiklund, and D. Liu, “Feasibility study of a core router based on a network on chip”, Proc of the Swedish System-on-Chip Conference (SSoCC), Tammsvik, Sweden, Apr 2005

26. J. Eilert and D. Liu, “Design of a Floating Point DSP for Full Precision MPEG-I Layer II and III Decoding”, Proc of the Swedish System-on-Chip Conference (SSoCC), Tammsvik, Sweden, Apr 2005

27. K. Folkesson, C. Svensson, B. Knuthammar and A. Dreyfert, “A High-Level Dynamic-Error Model of a Pipelined Analog-to-Digital Converter”, ISCAS 2005, Kobe, Japan, May 23-26, pp 5625-5628.

28. O. Flordal, D. Wu and D. Liu, “Accelerating CABAC Encoding for Multi-standard Media with Configurability”, accepted by IEEE 13th Reconfigurable Architectures Workshop (RAW) 2006.

29. H. Fredriksson and C. Svensson, “Mixed-Signal DFE for Multi-Drop, Gb/s, Memory Buses”. Swedish System-on-Chip Conference, 3 p., Tammsvik April 18-19, 2005.

30. H. Fredriksson and C. Svensson, “Blind Adaptive Mixed-Signal DFE for Gb/s, Multi-Drop”, accepted to VLSI-DAT’2006

31. D. González Muñoz, O. Gustafsson, and L. Wanhammar, "Evolution of filter order equations for linear-phase FIR filters using gene expression programming," National Conf. Radio Science (RVK), Linköping, Sweden, June 14-16, 2005, pp. 679-682.

32. O. Gustafsson, K. Johansson, and L. Wanhammar, "Optimization and quantization effects for sine and cosine computation using a sum of bitproducts," Asilomar Conf. Signals, Syst., Comp., Pacific Grove, CA, Oct. 30-Nov. 2, 2005.

33. O. Gustafsson, H. Ohlsson, and L. Wanhammar, "Carry-save adder based difference methods for multiple constant multiplication in high-speed FIR filters," National Conf. Radio Science (RVK), Linköping, Sweden, June 14-16, 2005, pp. 245-248.

34. O. Gustafsson and H. Ohlsson, "A low power decimation filter architecture for high-speed single-bit sigma-delta modulation," IEEE Int. Symp. Circuits Syst., Kobe, Japan, May 23-26, 2005.

35. M. Hansson, A. Alvandpour, S. K. Hsu and R. K. Krishnamurthy, “A process variation tolerant technique for sub-70nm latches and flip-flops”, 23rd Norchip Conference, Oulu, Finland, Nov 21-22, 2005, pp 149-152.

36. M. Hansson and A. Alvandpour, “Power-performance analysis of Sinusoidally clocked flip-flops”, 23rd Norchip Conference, Oulu, Finland, Nov 21-22, 2005, pp 153-156.

37. M. Hansson and A. Alvandpour, “Study of Sinusoidally Clocked Flip-Flops”. Swedish System on-Chip Conference, 4 p., Tammsvik April 18-19, 2005.

38. Z. He, G. Jervan, Z. Peng and P. Eles, "Power-Constrained Hybrid BIST Test Scheduling in an Abort-on-First-Fail Test Environment," Proc. 8th Euromicro Conference on Digital System Design (DSD'05), Porto, Portugal, Aug. 3-Sept. 3, 2005, pp. 83-86.

39. E. Hermanowicz and H. Johansson, "On designing minimax adjustable wideband fractional delay FIR filters using two-rate approach," in Proc. European Conf. Circuit Theory Design, Cork, Ireland, Aug. 29-Sept. 1, 2005.

40. U. Ingelsson, S. Goel, E. Larsson, and E. J. Marinissen, “Test Scheduling for Modular SOCs in an Abort-on-Fail Environment”, European Test Symposium (ETS'05), Tallinn, Estonia on May 22-25, 2005.

41. V. Izosimov, P. Pop, P. Eles and Z. Peng, "Design Optimization of Time- and Cost-Constrained Fault-Tolerant Distributed Embedded Systems," Proc. Design Automation and Test in Europe Conference (DATE'05), Munich, Germany, Mar. 7-11, 2005. **Best Paper Award.**

42. S. Jawed, M. Hartmann, H. Hauer, A. Alvandpour, " A 10-bit 250KHz Sigma-Delta Non-Uniform Quantization Analog-to-digital Converter", Radio Science and Communication conference, RVK, Linköping, June 14-16 2005, pp 275-280.

43. G. Jervan, R. Ubar, T. Shchenova and Z. Peng, "Energy Minimization for Hybrid BIST in a System-on-Chip Test Environment, Proc. IEEE European Test Symposium (ETS), Tallinn, Estonia, May 22-25, 2005, pp. 2-7.

44. G. Jervan, Z. Peng, R. Ubar and O. Korelina, "An Improved Estimation Technique for Hybrid BIST Test Set Generation," Proc. IEEE International Workshop on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Sopron, Hungary, Apr. 13-16, 2005, pp. 182-185.

45. K. Johansson, O. Gustafsson, and L. Wanhammar, "Low power architectures for sine and cosine computation using a sum of bit-products," Proc. IEEE NorChip Conf, Oulu, Finland, Nov. 21-22, 2005.

46. K. Johansson, O. Gustafsson, and L. Wanhammar, "A detailed complexity model for multiple constant multiplication and an algorithm to minimize the complexity," European Conf. Circuit Theory Design, Cork, Ireland, Aug. 29-Sept. 1, 2005.

47. K. Johansson, O. Gustafsson, A. G. Dempster, and L. Wanhammar, "Trade-offs in low power multiplier blocks using serial arithmetic," National Conf. Radio Science (RVK), Linköping, Sweden, June 14-16, 2005, pp. 271-274.

48. K. Johansson, O. Gustafsson, and L. Wanhammar, "Implementation of low-complexity FIR filters using serial arithmetic," IEEE Int. Symp. Circuits Syst., Kobe, Japan, May 23-26, 2005.

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