# Activity report on STRINGENT Research Center for 2003.

*Christer Svensson, Director*

## 1. General.

STRINGENT, Strategic Integrated Electronic Systems Research, was formed January 1st 2003 by joining 4 different groups (professor chairs) at Linköping University into a common research center. The four groups are Electronic Devices, Computer Engineering and Electronic Systems at Dept. of Electrical Engineering and Embedded Systems at Dept. of Computer Science.

### 1.1 Program description.

STRINGENT research program has formulated the vision:

*To make Circuit and System Sciences **lead** the development of future electronics.*

This vision will be accomplished by following goals:

New methods to convert complex ideas into silicon (*System Design)*
Improve efficiency of embedded systems (*Technology utilization*)
Reduce development times (*Design efficiency*)

The main goal during 2003 was to integrate the four groups into a common structure and to initiate cooperation among all researchers. As the overall goal is to create a strong research center, we consider the SSF support for STRINGENT as a base funding for the center, on top of which there are also other funding. We consider all activities in the center as its results and do not distinguish between results obtained through different funding (except when directly asked for by SSF). During 2003 we have successfully formed the center and had a common kick-off meeting. We have created a steering committee, which has met 4 times. We have created a scientific advisory board, which has met once. We have organized the center into 8 project groups across the original groups and departments, lead by 8 project group leaders, and created a steering and follow-up mechanism for the work in the groups. We have initialized marketing of the center to international industry. We are able to report a very successful first year of STRINGENT, with for example 4 dissertations, 10 licentiates, 1 book, 17 journal papers and 94 conference papers.

### 1.2 Project list.

The research program is organized in 8 project groups, lead by 8 project leaders. Each group is related to one of our overall goals, *System Design*, *Technology Utilization* and *Design Efficiency*. Ek, Da, Es and Em relates to the original research groups (professor chairs), Electronic devices, Computer Engineering , Electronic systems and Embedded systems.

**System design**
**Networks-on-chip (Dake Liu)**
Da1 SOCBUS
Em1 Optimization of real-time applications implemented on power constrained network-on-chip architectures
Em8 Heterogeneous networked embedded systems
Ek4 Global on-chip communication
**Heterogeneous multiprocessor systems (Olle Seger)**
Da2 Intra packet network processor
Da3 Low cost and low power audio decoder
Da4 Inter packet network processor
Da5 Low power base-band processor for SDR (Soft Defined Radio)
Em6 Design of heterogeneous multiprocessor systems for real-time applications
**Signal processing algorithms (Lars Wanhammar)**
Es4 Integrated active filters
Es5 Design and Implementation of Energy Efficient Digital Filters
Es6 Design and Implementation of Asymmetric Digital and Analog Filter Banks
Es7 Energy-efficient synchronization and equalization algorithms for multi-carrier systems
Es8 Low Power Algorithm Design and Implementation

**Technology utilization**

**High speed interfaces (Jerzy Dabrowski)**
Ek2 High speed off-chip communication
Ek5 Wide-band or tunable low noise amplifiers

**AD and DA converters (Mark Vesterbacka)**
Ek1 High performance AD conversion
Es1 CMOS digital-to-analog converters for communication
Es2 Algorithms and circuit techniques for increased performance of data Converters
Es3 High performance ADCs implemented in SOI technology

**High performance, low power circuit techniques (Atila Alvandpour)**
Ek7 System on chip clocking and communication
Ek8 Embedded memories

**Efficient design**

**Verification (Petru Eles)**
Ek3 Accurate models of AD-converters aimed for simulation
Em4 Formal verification of embedded systems in a reuse methodology
Em2 Modeling and verification of embedded systems

**Testing (Zebo Peng)**
Ek6 Testability-oriented design techniques for mixed-signal/RF integrated circuits
Em3 Hybrid BIST methodology for complex electronic systems
Em5 Testing system-on-chips using functional bus
Em7 Built-in self-test for ASICs and SoCs
Em9 SoC wrapper design, TAM configuration and test scheduling

## 2 Graduate education.

### 2.1 Graduate students

31 graduate students participate in STRINGENT, of which 18 are funded by the STRINGENT program (with an average funding of 75%). For a full list of students, see below. For a list of students financed through SSF, see form 4.

Ila Andersson
Stefan Andersson
Alexandru Andrei
Erik Backenius
Håkan Bengtsson
Peter Caputa
L A Cortes
Kalle Folkesson
Henrik Fredriksson
Martin Hansson
Tomas Henriksson
Emil Hjalmarsson
Robert Hägglund
Darius Jakonis
Gert Jervan
Daniel Karlsson
Anders Larsson
Weidong Li
Ulf Nordqvist
Sorin Manolache
Abdil Rashid Mohamed
Mikael Olausson
Henrik Olsson
Mattias Olsson
Paul Pop
Traian Pop
Linnea Rosenbaum
Sumant Sathe
Erik Säll
Erik Tell
Daniel Wiklund

### 2.2 Graduate courses

8 Ph.D. courses was given during 2003. Additionally, Stringent arranged a summer school for all Swedish students in the field, see 4.3.

Advanced DSP architecure (Dake Liu)

Introduction to network processors (Dake Liu)

Real-time and embedded systems (Zebo Peng)

Distributed systems (Petru Eles)

Formal modeling and verification for RT systems (Petru Eles)

Heuristic algorithms for combinatorial optimization problems (Zebo Peng)

SOI CMOS circuits (Mark Vesterbacka)

DSP for music and audio (Mark Vesterbacka)

### 2.3 Theses.

During 2003 we produced 4 doctors and 10 licentiates, see below.

Thomas Henriksson, "Intra-Packet Data-flow protocol processor", Ph.D. May 2003 (Stringent funding of total education: 12%). Now working for Philips, Eindhoven, The Netherlands.

Oscar Gustafsson, "Contributions to Low-Complexity Digital Filters", Ph.D. Sept. 2003. (Stringent funding of total education: 0%). Working at the department.

Paul Pop, "Analysis and Synthesis of Communication-Insensitive Heterogeneous Real-Time Systems", Ph.D. (Stringent funding of total education: 10%). Working at the department.

Annika Rantzner, "Photo diodes for machine vision", Ph.D. March 2003 (Stringent funding of total education: 0%). Working with Integrated Vision Products, Linköping.

W. Li, "Studies on Implementation of Low Power FFT Processors", Licentiate, 2003. (Stringent funding of total education: 16%).

H. Ohlsson, "Studies on implementation of Digital Filters with High Throughput and Low Power Consumption", Licentiate, June 2003. (Stringent funding of total education: 16%).

L. Rosenbaum, "Contributions to Low-Complexity Maximally Decimated Filter Banks", Licentiate, Sept. 2003. (Stringent funding of total education: 3%).

R. Hägglund, "Studies on Design Automation of Analog Circuits – Performance Metrics", Licentiate, Dec. 2003. (Stringent funding of total education: 16%).

E. Hjalmarsson, "Studies on Design Automation of Analog Circuits – The Design Flow", Licentiate, Dec. 2003. (Stringent funding of total education: 16%).

Traian Pop, "Scheduling and Optimization of Heterogeneous Time/Event-Triggered Distributed Embedded Systems", Licentiate, June 2003 (Stringent funding of total education: 0%).

Daniel Karlsson, "Towards Formal Verification in a Component-Based Reuse Methodology", Licentiate, December 2003. (Stringent funding of total education: 16%).

K. Folkesson, "ADC modeling for system simulation", Licentiate, June 2003 (Stringent funding of total education: 16%).

D Wiklund, "An on-chip network architecture for hard real-time systems", Licentiate, January 2003 (Stringent funding of total education: 10%).

U. Nordqvist, "A programmable network interface accelerator", Licentiate, January 2003 (Stringent funding of total education: 17%).

## 3. Research

### 3.1 Participating researchers.

18 persons except students are engaged in STRINGENT, of whom 8 are partly funded by the program (with an average funding of 21%, see form 5). Participating researchers are:

Prof. Atila Alvandpour
Dr Jertzy Dabrovski
Prof. Petru Eles
Dr Håkan Johansson
Dr. Erik Larsson
Prof. Dake Liu
Dr. Per Löwenborg
Dr Kent Palmkvist
Prof. Zebo Peng
Dr. Olle Seger
Prof. Christer Svensson
Dr. Ingemar Söderquist
Prof. Mark Vesterbacka
Prof. Lars Wanhammar

### 3.2 Publications.

The Research activity during 2003 has resulted in one book, 17 papers in scientific journals, 3 book chapters, and 94 papers in scientific conferences, of which 3 were invited. 5 silicon chips has been taped out and 4 have been evaluated. No patents or patent applications were reported. For a publication list, see Appendix 1.

## 4. External activities.

### 4.1 Cooperation with Swedish industry.

One of the groups participates with Volvo AB in an EU excellence center, Artist.

A workshop was arranged with Infineon, "ADDA workshop", Jan. 29, 2003.

A workshop was arranged with Ericsson, "LNA workshop", Nov. 3, 2003.

### 4.2 Cooperation with foreign industry.

We have three research grants from foreign industry, 50kUSD from Intel (USA), 75kUSD from Intel (USA), Infineon (Germany) and Samsung (Korea), and 75 kUSD from Winbond (Taiwan).

### 4.3 Cooperation with other Swedish programs.

A national conference, SSoCC was arranged April 8-9 in Falkenberg in cooperation with Socware and FlexSoC.

A national summer school, Intelect, was arranged in Örebro in cooperation with Socware, August 25-17, 2003.

A workshop was arranged with Vinnova, "Hardware Platforms for Future Networks", Nov. 21, 2003

We have a close cooperation with the Socware program, including a funding of 3800 ksek (7000ksek promised).

One EU program with Infineon and CTH, Super-ADC, was funded by 22 keuro.

### 4.4 Webpage

The webpage is found at http://www.ida.liu.se/~eslab/stringent/. Responsible person is Erik Larsson (erila@ida.liu.se).

### 4.5 Information about the program.

We arranged a presentation of STRINGENT at Infineon, Munich, June 17, which hopefully will give rise to closer cooperation. We expect to continue with presentations at other industry during 2004, for example Ericsson Mobile Platforms (Sweden) and Philips (The Netherlands).

We plan publicity through Swedish technical press during 2004.

## 5. Program administration.

The program has been managed by the program director, prof. Christer Svensson, with support from assistant Anna Folkesson

### 5.1 Steering committee.

The Steering committee has met 4 times during 2003. The members are:

Magnus Danestig, Acreo, chairman (magnus.danestig@acro.se)
Jan Grahn, CTH (jan.grahn@ep.chalmers.se)
Jonas Plantin, Ericsson (jonas.plantin@ericsson.com)
Mikael Rudberg, Infineon (mikael.rudberg@infineon.com)
Lars Svensson, CTH (larssv@ce.chalmers.se)

5.2 Advisory board.

The Advisory board has met once during 2003. The members are:

Shekhar Borkar, Intel, USA (Shekhar.y.borkar@intel.com)
Manfred Glesner, T U Darmstadt, Germany (glesner@mes.tu-darmstadt.de)
Gunnar Björklund, Infineon, Sweden (gunnar.bjorklund@mic.ericsson.se)
Christain Piguet, CSEM, Switzerland (christian.piguet@csem.ch)
Tor Ramstad, NTNU, Norway (tor@tele.ntnu.no)

Linköping, March 26, 2004,

Magnus Danestig — Chairman
Christer Svensson — Director

***STRINGENT 2003, Appendix 1, Publications***

**Journals**

1. NU Andersson, KO Andersson, JJ Wikner, M Vesterbacka: "Models and implementation of a dynamic element matching DAC", Kluwer Int. journal of analog integrated circuits and signal processing, vol 34, No 1, pp 7-16, Jan 2003.
2. LA Cortes, P Eles, Z Peng: "Modeling and formal verification of embedded systems based on a petri net representation", Journal of System Architectures, vol 49, no. 12-15, pp. 571-598, Dec 2003.
3. E Elias, P Löwenborg, H Johansson, L Wanhammar: "Tree-structured IRR/FIR uniform-band and octave-band filter banks with very low-complexity analysis or synthesis filters", to appear in EURASIP Sign. Proc.
4. O. Gustafsson, H Johansson, L Wanhammar: "Single filter frequency masking high-speed recursive digital filters", Circuits, Syst., Signal Processing, vol 22, No 2, pp 219-238, 2003.
5. S Hsu, A Alvandpour, S Mathew, S Lu, R Krishnamurthy, S Borkar: "A 4.5 GHz 130nm 32-kb LO cache with a leakage-tolerant self reverse-bias bitline scheme", IEEE Journal of Solid-State Circuits, Vol 38, No. 5, May, pp 755-761, 2003.
6. H Johansson: "Multirate IRR filter structures for arbitrary bandwidths", accepted for publication in IEEE Trans. Circuits Syst. I, vol 50, No 12, pp. 1515-1529, Dec 2003.
7. H Johansson, P Löwenborg: "On the design of adjustable fractional delay FIR filters", IEEE Trans Circuits Syst. II, vol 50, No 4, pp 164-169, April 2003.
8. H Johansson, P Löwenborg: "On linear-phase FIR filters with variable bandwidth", accepted for publication in IEEE Trans. Circuits Syst. I.
9. H Johansson, T Saramäki: "Two-channel FIR filter banks utilizing the frequency-response masking approach", Circuits, Syst., Signal Processing, vol 22, No 2, pp 157-192, 2003.
10. R. Jonsson, Q. Wahab, S. Rudner and C. Svensson, "Computational load pull simulations of SiC microwave power transistors", Solid-State Electronics, vol. 47, pp. 1921-1926, 2003.
11. E Larsson, K Arvidsson, H Fujiwara, Z Peng: "Efficient test solutions for core-based design", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems.
12. P Löwenborg, H Johansson, L Wanhammar: "Two-channel digital and hybrid analog/digital multirate filter banks with very low complexity analysis or synthesis filters", IEEE Trans. Circuits Sys II, Vol 50, No. 7, pp 355-367, July 2003.
13. P Löwenborg, H Johansson, L Wanhammar: "First-order sensitivity of complementary diplexers", accepted for publication in IEEE Trans. Circuits Syst. I.
14. P Pop, P Eles, Z Peng: "Schedulability analysis and optimization for the synthesis of multi-cluster distributed embedded systems", IEEE Proceedings – Computer & Digital Techniques, (accepted for publication).
15. T Saramäki, J Yli-Kaakinen, H Johansson: "Optimization of frequency-response-masking base FIR filters", accepted for publiction in J. Circuits, Syst. Comput.
16. I Söderquist: "Globally updated mesochronous design style", IEEE Journal of Solid State Circuits, vol 38, No. 7, pp 1242-1249, July, 2003.

**Conferences**

1. A Alvandpour, R Krishnamurthy, D Eckerbert, S Apperson, B Bloechel, S Borkar: "A 3.5 GHz 32mW 150nm multiphase clock generator for high-performance microprocessors", IEEE Int. solid-state circuits conference, pp 112-113, Feb 9, 2003.

2. A Alvandpour, D Somasekhar, R Krishnamurthy, V De, S Borkar, C Svensson: “Bitline leakage equalization for sub-100nm caches” to be presented at ESSCIRC, Estoril, Portugal,pp 401-404, Nov 16-18, 2003.
3. KO Andersson, NU Andersson, M Vesterbacka, JJ Wikner: “A method of segmenting digital-to-analog converters”, Proc. IEEE Southwest symposium on mixed-signal design, Las Vegas, USA, pp 32-37, Feb 23-25, 2003.
4. KO Andersson, NU Andersson, M Vesterbacka, JJ Wikner: “A 14-bit dual current-steering DAC”. Prov SSoCC´03, Eskilstuna, Sweden, April 8-9, 2003.
5. KO Andersson, M Vesterbacka: “Partial decomposition of digital-to-analog converters”, to appear in Proc. IEEE Mediterranean Electrotechnical Conf., Dubrovnik, Croatia, May 12-15, 2004.
6. S Andersson, C Svensson: “An active recursive RF filter in 0.35 um BiCMOS”, The GigaHerz symposium, Linköping, November 2003.
7. S Andersson, C Svensson, O Drugge: “Wideband LNA for a multistandard wireless receiver in 0.18 um CMOS”, ESSCIRC´2003, Estoril, Portugal, Sept 16-18,2003.
8. E Backenius, M Vesterbacka: “Characteristics of a differential D flip-flop”, Proc SSoCC´03, Eskilstuna, Sweden, April 8-9, 2003.
9. E Backenius, M Vesterbacka: “Design of circuits for a robust clocking scheme”, to appear in Proc. IEEE Mediterranean Electrotechnical conference, Dubrovnik, Croatia, May 12-15, 2004.
10. H Bengtsson, C Svensson: ”Speed study of a 2.5 Gb/s equalizer for optical communication in a 3 V 0.35 um CMOS process”, Proc SSoCC´03, Eskilstuna, April 8-9, 2003.
11. J Carlsson, W Li, K Palmkvist, L Wanhammar, S Zhuang: “A design path for design of GAL based communcation systems”, Proc. Swedish system-on-chip conference, Eskilstuna, Sweden, April 8-9, 2003.
12. J Carlsson, K Palmkvist, L Wanhammar: “An 8-by-8 point 2D processor based on the GALS approach”, Proc. Of IEEE NorChip conf, Riga, Latvia, Nov 10-11, 2003.
13. LA Cortes, P Eles, Z Peng: “Quasi-static scheduling for real-time systems with hard and soft tasks”, accepted for Design, Automation and Test in Europe (DATE 2004), Paris France, February 16-20, 2004.
14. LA Cortes, P Eles, Z Peng: “Static scheduling of monoprocessor real time systems composed of hard and soft tasks”, accepted for The IEEE Int. workshop on Electronic Design, Test and Applications (DELTA 2004), Perth, Australia, January 28-30, 2004.
15. J Dabrowski: “BiST model for IC RF-transceiver front-end”, 18th Int. symposium on defect and fault tolerance in VLSI systems, Cambridge, MA, USA, Nov 3-5, 2003.
16. J Dabrowski: “Fault modeling of RF blocks based on noise analysis”, accepted to ISCAS´04, Vancouver, Canada, May 23-26, 2004
17. J Dabrowski: “Loopback BiST for RF front-ends in digital transceivers”, Int. symposium on SoC, Tampere, Finland, Nov 19-21, 2003.
18. J Dabrowski, L Li: “Signal path sensitization for BiST in integrated RF transceivers”, accepted to DDECS´04.
19. AG Dempster, O Gustafsson, JO Coleman: “Towards an algorithm for matrix multiplier blocks”, Proc European conference circuit theory design, Krakow, Poland, Sept 2003.
20. H Eriksson, T Henriksson, P Larsson-Edefors, C Svensson: “Full-custom vs. standard-cell design flow - An adder case study”, Proc of Asia South Pacific design automation conference, Kitakyushu, Japan, pp 507-510, Jan 2003.
21. K Folkesson, D Jakonis, C Svensson: “A jitter measurement technique for high-speed sampling systems”, SSoCC´03, Eskilstuna, April 8-9 2003.
22. K Folkesson, C Svensson: “An accurate ADC model in radar system simulation”, IWADC conference, Perugia, Italy, pp 25-28, Sept 2003.

23. O Gustafsson, H Ohlsson, M Mohsen, L Wanhammar: “Implementation of high-speed single filter frequency-response masking recursive filters”, Proc. Of IEEE NorChip conf, Riga, Latvia, Nov 10-11, 2003.
24. M Hansson, A Alvandpour: “Crosstalk analysis considering power and delay on interconnects”, NorChip Conference, Riga, Latvia, Nov 10-11, 2003.
25. T Henriksson, D Liu: “Implementation of fast CRC calculation”, Proc. of Asia South Pacific design automation conference, Kitakyushu, Japan, pp 563-564, Jan 2003.
26. T Henriksson, D Wiklund, D Liu: “VLSI implementation of a switch for on-chip networks”, Proc. Of Int workshop DDECS, Poznan, Poland, April 2003.
27. E Hjalmarson, R Hägglund, L Wanhammar: “A design platform for computer-aided design of analog amplifiers”, Proc SSoCC´03, Eskilstuna, Sweden, 8-9 April, 2003
28. E Hjalmarson, R Hägglund, L Wanhammar: “An equation-based optimization approach for analog circuit design”, Proc Int. Symp on Signals, Circuits & Systems, Iasi, Romania, July 2003.
29. E Hjalmarson, R Hägglund, L Wanhammar: “An optimization-based approach for analog circuit design”, Proc European conference on circuit theory and design, Krakow, Poland, Sept 2003.
30. E Hjalmarson, R Hägglund, L Wanhammar: “Optimization-based design space exploration on analog circuits”, Proc European conference on circuit theory and design, Krakow, Poland, Sept 2003.
31. S Hsu, B Chatterjee, M Sachdev, A Alvandpour, R Krishnamurthy, S Borkar: “A 90nm 6.5 GHz 256x64b dual supply register file with split decoder scheme”, Int. symposium on VLSI circuits, pp 237-238, 2003.
32. R Hägglund, E Hjalmarson, L Wanhammar: „Using optimization to find design trade-offs in analog amplifier design”, Proc of SSoCC´03, Eskilstuna, Sweden, April 8-9, 2003.
33. D Jakonis, J Dabrowski, C Svensson: “Noise analysis of downversion sampling mixer”, accepted to ECCTD, Krakow, Poland, 2003.
34. D Jakonis, J Dabrowski, C Svensson: “Noise reduction by sampling frequency choice in subsampling mixer”, Proc of SSoCC´03, Eskilstuna, Sweden, April 8-9, 2003.
35. D Jakonis, K Folkesson, J Dabrowski, C Svensson: “Downconversion sampling mixer for wideband low-IF receiver”, Proc of MIXDES, pp 208-213, Lodz, Poland, 2003.
36. D Jakonis, C Svensson: “A 1.6 GHz downconversion sampling mixer in CMOS”, Proc of IEEE ISCAS, vol 1, Bangkok, Thailand, pp 725-728, 2003.
37. G Jervan, P Eles, Z Peng, R Ubar, M Jenihhin: “Hybrid BIST time minimization for core-based systems with STUMPS architecture”, Proc 18$^{th}$ Int. symposium on defect and fault tolerance in VLSI systems (DFT), Cambridge, Mass, USA, Nov 3-5, 2003.
38. G Jervan, P Eles, Z Peng, R Ubar, M Jenihhin: “Test time minimization for hybrid BIST of core-based systems”, Proc. 12$^{th}$ IEEE Asian test symposium (ATS), Xian, China, Nov 17-19, 2003.
39. H Johansson: “Efficient frequency-response-masking based FIR filter structures for inter-polation and decimation”, Third Int. workshop Spectral methods multirate signal processing, Barcelona, Spain, Sept 13-14, 2003.
40. H Johansson: “On lowpass and highpass IIR filters with an adjustable bandwidth”, European conf Circuit Theory Design, Krakow, Poland, Sept 1-4, 2003.
41. H Johansson, P Löwenberg: “Linear programming design of linear-phase FIR filters with variable bandwidth”, Proc IEEE Symp. Circuits Syst., Bangkok, Thailand, May 25-28, 2003.
42. K Johansson, O Gustafsson, L Wanhammar: “Switching activity in bit-serial constant coefficient serial/parallel multipliers”, Proc of IEEE NorChip conf, Riga, Latvia, Nov 10-11, 2003.

43. R Johansson, L Lindgren, J Melander, B Möller: "A multi-resolution 100 GOP S4 Gpixels/s programmable CMOS imge sensor for machine vision" IEEE workshop on charge coupled devices and advanced image sensors, 2003.

44. D Karlsson, P Eles, Z Peng: "Automatic generation of a formal verification bench for a reuse methodology", SSoCC´03, Eskilstuna, April 8-9, 2003.

45. M Karlsson, M Vesterbacka: "A non-overlapping two-phase clock generator with adjustable duty cycle", To apprear in Proc GigaNertz 2003 Symp., Linköping, Sweden, Nov 4-5, 2003.

46. M Karlsson, M Vesterbacka: " A robust non-overlapping two-phase clock generator", Proc SSoCC´03, Eskilstuna, Sweden, April 8-9, 2003.

47. M Karlsson, M Vesterbacka, W Kulesza: " Design of digit-serial pipelines with merged logic and latches", Proc. Norchip 2003, Riga, Latvia,pp. 68-71, Nov 10-11, 2003.

48. M Karlsson, M Vesterbacka, M Kulesza: "Ripple-carry versus carry-look-ahead digit-serial adders", Proc Norchip 2003, Riga, Latvia, pp. 264-267, Nov 10-11, 2003.

49. M Karlsson, M Vesterbacka, W Kulesza: " A method for increasing the throughput of fixed coefficient digit-serial/parallel multipliers", to appear in Proc. 2004 IEEE Int. Symp on Circuits and Systems, ISCAS´04, Vancouver, Canada, May 23-26, 2004.

50. CH Kim, K Roy, S Hsu, A Alvandpour, R Krishnamurthy, S Borkar: "A process variation compensating technique for sub-90nm dynamic circuits", Int. symposium on VLSI circuits, pp 205-206, 2003.

51. K Ladernäs, J Holmberg, M Vesterbacka: "A high-speed low-latency digit-serial hybrid adder". To appear in Proc. 2004 IEEE Int. Symp. On Circuits and Systems, ISCAS´04, Vancouver, Canada, May 23-26, 2004.

52. A Larsson, E Larsson, P Eles, Z Peng: "Buffer and controller minimisation for time-constrained testing of system-on-chip", Proc 18th Int. symposium on defect and fault tolerance in VLSI systems (DFT), Cambridge, Mass, USA, Nov 3-5, 2003.

53. E Larsson, H Fujiwara: "Test resoruce partitioning and optimization for SOC designs, IEEE VLSI Test Symposium (VTS`03), Napa, USA, April 27–May 1, 2003.

54. E Larsson, Z Peng: "A reconfigurable power-conscious core wrapper and its application to SOC test scheduling", IEEE Int. test conference (ITC´03), Charlotte, NC, USA, September 30-Oct 2, 2003.

55. E Larsson, J Pouget, Z Peng: "System-on-chip test scheduling based on defect probability", Int. test synthesis workshop (ITSW), Santa Barbara, CA, USA, March 31-April 2, 2003.

56. E Larsson, J Pouget, Z Peng: "Defect probability-based system-on-chip test scheduling", Proc. 6th IEEE international workshop on design and diagnostics of electronics circuits and systems (DDECS´03), Poznan, Poland, April 14-16, 2003.

57. W Li, J Carlsson, J Claeson, L Wanhammar: "A GALS based 16-point pipeline FFT core", Proc. Of IEEE NorChip conf, Riga, Latvia, Nov 10-11, 2003.

58. W Li, L Wanhammar: "Low power design for data dependence", Proc SSoCC´03, Eskilstuna, Sweden, April 8-9, 2003.

59. P Löwenborg, H Johansson: "Analysis of continuous-time-input A/D modulators and their generalizations", Eur conf Circuit Theory Design, Krakow, Poland, Sept 1-4, 2003.

60. S Natarajan, A Alvandpour: "High performance and SER insensitive memories", SPIE´s International Symposium on Microelectronics, MEMS, and Nanotechnology, Dec 9-12, 2003.

61. S Natarajan, A Alvandpour: "Ultra low power ferroelectric memories for SoC´s", SPIE´s International Symposium on Microelectronics, MEMS, and Nanotechnology, Dec 9-12, 2003.

62. S Natarajan, A Alvandpour: "SoC versus SIP: What makes sense?", SPIE´s International Symposium on Microelectronics, MEMS, and Nanotechnology, Dec 9-12, 2003.

63. U Nordqvist: "Power efficient packet buffering in a protocol processor", Swedish system-on-chip conference (SSoCC´03), Eskilstuna, Sweden, April 8-9, 2003.

64. U Nordqvist, D Liu: "Packet classification and termination in a protocol processor", HPCA9 workshop on network processor, Anaheim, USA, pp 88-99, Feb 2003.
65. U Nordqvist, D Liu: "Control path in a protocol processor", Proc of Midwest symposium on circuits and systems (MWCAS), Cairo, Egypt, December 2003.
66. U Nordqvist, D Liu: "Power optimized packet buffering in a protocol processor", Proc of Int. conference on electronic circuits and systems (ICECS), Sharjag, United Arab Emirates, December 2003.
67. H Ohlsson, O Gustafsson, W Li, L Wanhammar: "An environment for design and implementation of energy efficient digital filters", Proc. SSoCC´03, Eskilstuna, Sweden, April 8-9, 2003.
68. H Ohlsson, W Li, D Capello, L Wanhammar: "Design and implementation of an SRAM layout generator", Proc. Of IEEE NorChip conf, Riga, Latvia, Nov 10-11, 2003.
69. M Olsson: "Implementation of an IEEE802.11a syncronizer", Proc SSoCC´03, Eskilstuna, Sweden, April 8-9, 2003.
70. ST Oskuii, A Alvandpour: "A comparative study on low power, high performance standard cell Flip Flops", SPIE´s International Symposium on Microelectronics, MEMS, and Nanotechnology, Dec. 9-12, 2003.
71. Z Peng: "System-on-chip test optimization", Proc. International East-west design & test conference (EWDTC), Alushta, Ukraine, Sept 17-21, 2003.
72. T Pop, P Eles, Z Peng: "Design optimization of mixed time/event-triggered distributed embedded systems", Proceedings of the IEEE/ACM/IFIP international conference on HW/SW codesign and system synthesis (CODES+ISSS 2003), Newport Beach, California 2003, (accepted for publication).
73. T Pop, P Eles, Z Peng: "Schedulability analysis for distributed heterogeneous time/event-triggered real-time systems", Proceedings of the 15th Euromicro conference on real-time systems, Porto, Portugal, pp 257-266, 2003.
74. P Pop, P Eles, Z Peng: "Schedulability analysis and optimization for the synthesis of multi-cluster distributed embedded systems", Proceedings of Design, Automation & Test in Europe conference, , Munich, Germany, pp 184-189, 2003.
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76. J Pouget, E Larsson, Z Peng, M-L Flottes, B Rouzeyre: "An efficient approach to SoC wrapper design, TAM configuration and test scheduling, Proc. European test workshop (ETW), Maastricht, The Netherlands, May 25-28, 2003.
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