Assessing Feasibility of Static WCET Analysis for Industry-strength Applications

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Description

Hard real-time applications require absolute guarantees in their execution time. Failures to meet such guarantees may lead to catastrophic effects, often costing human lives. Worst-case execution time (WCET) captures the execution time of a program over all inputs. As a result, the WCET metric can be used to provide hard real-time guarantees for a program. Nevertheless, unfortunately, enumerating all inputs of a program is potentially *infeasible*. Therefore, researchers have looked into static WCET analysis methodologies. The idea is to statically analyze a program and the underlying micro-architecture, independent of program inputs.

The project will assess the feasibility of static WCET analysis techniques. Although a significant research has been put forward for statically analyzing WCET, their feasibility in the context of industry-strength processors (and applications) remain ambiguous. In this project, we shall investigate the efficiency and precision of static analyzers in the context of computing the WCET of a program. The project will be carried out in collaboration with SAAB Aeronautics, Linköping and it is due to start by August, 2015.

Plan

To accomplish the goal of this project, we aim to proceed as follows:

1. Gain familiarity with the latest works on static WCET analysis techniques, as implemented in commercial tool `aiT` [1] and academic tools such as `Chronos` [2]. In particular, understand a few seminal works on micro-architectural modeling to bound the timing delay caused by the underlying platform.
2. Understand the micro-architecture (*e.g.* caches and pipeline) of a processor used for an industry-strength, hard real-time application. Such an application and the processor are used in SAAB Aeronautics.
3. Check whether existing analysis techniques can be employed to model the micro-architecture of the processor used in SAAB. Incorporate appropriate changes in the analysis to model the micro-architecture.

Once the preceding stage is finished, the project aims to do the following:

1. Leverage on recent developments in static WCET analysis to model the micro-architecture of a real processor (used in the industry).
2. Compare the analysis efficiency and precision with the measurement, which is the *state-of-the-art* technique used in most industries.

Qualification

This 30 hp thesis will be carried by one Masters student.

- The student should have very good programming skills.
- The student should have taken a compilers and a computer architecture course.
- Good background in discrete mathematics and logic are a plus.

References

1. aiT AbsInt. `http://www.absint.com/ait`.
2. Xianfeng Li, Yun Liang, Tulika Mitra, and Abhik Roychoudhury. Chronos: A timing analyzer for embedded software. *Science of Computer Programming*, 2007. `http://www.comp.nus.edu.sg/~rpembed/chronos`.