

Test Design for Computer Systems with Life-Time Perspective

Project 05.06

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1. Introduction and Project description

While it is possible to manufacture integrated circuits (ICs) with billions of transistors, it is a major challenge to ensure fault-free ICs. ICs can be defective already at manufacturing or become defective while in operation. The objective of this project is to find test schemes that can be used through the life-time of a system.

The main achievement in this project is a novel architecture to be used in manufacturing test. The architecture has been rewarded by the Institution of Engineering and Technology (IET) Premium Award and currently Intel is testing some of their processors with the scheme.

The plan for next year is to start to integrate the work in this project with the currently accepted FP7 project. We plan to explore the usage of the developed architecture at in-field test and diagnosis. The short-term plan is: (1) finalize the collaborating with Bart Vermeulen and Kees Goossens on silicon debug/diagnosis through the SSF funding, (2) continue the collaboration with Dr. Virendra Singh at Indian Institute of Science, and (3) establish contact with the partners in the FP7 project, that is University of Tallinn, Bremen and Graz as well IBM, Ericsson, TransEDA and Testonica.

2. Results

The result from the project is summarized below.

- **Awards:** (1) The Institution of Engineering and Technology (IET) Premium Award, 2009, for the paper "Architecture for Integrated Test Data Compression and Abort-on-Fail Testing in a Multi-Site Environment" by Erik Larsson. (2) Supervisor for Dan Adolfsson, Improved Scan Chain Diagnosis, winner of "Lilla Polhemspriset", 2008.
- **Ph D students:** (1) Anders Larsson Ph. D. as of November 2009. (2) Dimitar Nikolov, Ph D student from april 2009. Funded by FP7 project. (3) Mudassar Majeed, becoming Ph.D student shortly. Funded by HEC (Pakistan).
- **Post doc:** Urban Ingelsson, from September 1 2009. Funded by FP7 project.
- **Funding:** (1) FP7 (ICT-2009-4) - Diagnosis and Model-Based Debug in Embedded Systems Design (DIAMOND), 2010-2013, (2) SSF - 12-months visit to NXP Semiconductors (Netherlands), 2008-2010, (3) STINT support for collaboration with Indian Institute of Science, Bangalore, 2008-2011, and (4) scholarship from Ericsson AB, 2007.

2.1 Partners

- Gunnar Carlsson (Ericsson, Stockholm, Sweden) and Erik Jan Marinissen, Sandeep Kumar Goel, Mohamed Azimane, Paul Wielage, and Clemens Wouters (NXP Semiconductors, Eindhoven, The Netherlands).
- Krishendu Chakrabarty, Duke University, USA, Virendra Singh, Indian Institute of Science, India, and Hideo Fujiwara, Nara Institute of Science and Technology, Japan.

3. CENIIT co-operations

In co-operation with Dr Jerzy Dabrowski (project leader of 03.03), a PhD course was given 2007 and is scheduled to be repeated. We are also working with Dr Dabrowski to establish the Swedish Network of Design for Test Research (SNDFT).

4. Budget

- Spending for the first, second and third year was as follows for each year: Erik Larsson (40%) 222 kkr, Anders Larsson (Ph.D student) (30%) 126 kkr, Travel 30 kkr, Overhead including tax 72 kkr. TOTAL per year 450 kkr.
- Spending for the fourth year was as follows: Erik Larsson (40%) 222 kkr, Dimitar Nikolov (scholarship-prospective Ph.D student) (100%) 126 kkr, Travel 30 kkr, Overhead including tax 72 kkr. TOTAL per year 450 kkr.
- Spending for the fifth year is as follows: Erik Larsson (40%) 222 kkr, Dimitar Nikolov (Ph.D student) (30%) 126 kkr, Travel 30 kkr, Overhead including tax 72 kkr. TOTAL per year 450 kkr.

5. Publications

During November 2004 to October 2009, we have 54 publications distributed as follows: 1 book, 3 book chapters, 8 journal

publications, 18 conference/symposium papers, and 22 workshop papers.

5.1 Books and Book Chapters

- [1] Erik Larsson and C.P. Ravikumar, Power-Aware System-Level DFT and Test Planning, Power-Aware Testing and Test Strategies for Low Power Devices, Patrick Girard, Nicola Nicolici, Xiaoqing Wen (Eds.), 2009, ISBN: 978-1-4419-0927-5.
- [2] Erik Larsson and Zebo Peng, An Integrated System-on-Chip Test Framework, Design, Automation, and Test in Europe, The Most Influential Papers of 10 Years DATE, Lauwereins, Rudy; Madsen, Jan (Eds.), 2008, pages 439-454, ISBN: 978-1-4020-6487-6.
- [3] Erik Larsson and Stina Edbom, Combined Test Data Selection and Scheduling for Test Quality Optimization under ATE Memory Depth Constraint, Selected papers from IFIP VLSI-SoC, 2005.
- [4] Erik Larsson, Introduction to Advanced System-on-Chip Test Design and Optimization , FRONTIERS IN ELECTRONIC TESTING: Volume 29, Springer, ISBN: 1-4020-3207-2, May 2005.

5.2 Journals

- [5] Erik Larsson, An Architecture for Integrated Test Data Compression and Abort-on-Fail Testing in a Multi-Site Environment , IET Computers & Digital Techniques, July 2008, Volume 2, Issue 4 pages 275-284.
- [6] Erik Larsson and Zebo Peng, A Reconfigurable Power Conscious Core Wrapper and its Application to System-on-Chip Test Scheduling , Journal of Electronic Testing: Theory and Application
- [7] Soheil Samii, Mikko Selkälä, Erik Larsson, Krishnendu Chakrabarty, and Zebo Peng, Cycle-Accurate Test Power Modeling and its Application to SoC Test Architecture Design and Scheduling, IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, Volume 27, Issue 5, May 2008 Page(s):973 - 977
- [8] Erik Larsson and Stina Edbom, Test Data Truncation for Test Quality Maximization under ATE Memory Depth Constraint, IET Computers & Digital Techniques, Volume 1, Issue 1, January 2007, pages 27-37.
- [9] Erik Larsson and Hideo Fujiwara, System-on-Chip Test Scheduling with Reconfigurable Core Wrappers, Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 14, No. 3, March 2006.
- [10] Erik Larsson and Zebo Peng, Power-Aware Test Planning in the Early System-On-Chip Design Exploration Process, Transactions on Computers, Volume 6, Number 2, February 2006, pages 227-239.
- [11] Erik Larsson, Julien Pouget, and Zebo Peng, Abort-on-Fail Based Test Scheduling, JETTA Journal of Electronic Testing; Theory and Applications (JETTA), Volume 21, Number 6, December 2005, pages 651 - 658.
- [12] Julien Pouget, Erik Larsson, and Zebo Peng, Multiple Constraints Driven System-on-Chip Test Time Optimization, JETTA Journal of Electronic Testing; Theory and Applications (JETTA), Volume 21, Number 6, December 2005, pages 599-611.

5.3 Conferences

- [13] Dan Adolfsson, Joanna Siew, Erik Jan Marinissen, Erik Larsson, On Scan Chain Diagnosis for Intermittent Faults, IEEE Asian Test Symposium (ATS), Taichung, Taiwan, November, 2009.
- [14] Jaynarayan T Tudu, Erik Larsson, Virendra Singh, and Adit Singh, Capture Power Reduction for Modular System-on-Chip Test, IEEE/VSI VLSI Design and Test Symposium (VDAT), Bangalore, India, July, 2009.
- [15] Jaynarayan T Tudu, Erik Larsson, Virendra Singh, and Vishwani Agrawal, On minimization of peak power for scan circuit during test, European Test Symposium (ETS 2009), Sevilla, Spain, May, 2009.
- [16] Mikael Väyrynen, Virendra Singh, and Erik Larsson, Fault-Tolerant Average Execution Time Optimization for General-Purpose Multi-Processor System-on-Chips, Design Automation and Test in Europe (DATE 2009), Nice, France, April, 2009.
- [17] Anders Larsson, Xin Zhang, Erik Larsson, and Krishnendu Chakrabarty, Core-Level Expansion of Compressed Test Patterns, Asian Test Symposium (ATS 2008), Sapporo, Japan, November 24-27, 2008.
- [18] Anders Larsson, Erik Larsson, Krishnendu Chakrabarty, Petru Eles, and Zebo Peng, Test-Architecture Optimization and Test Scheduling for SOCs with Core-Level Expansion of Compressed Test Patterns, Design, Automation, and Test in Europe (DATE 2008) Munich, Germany, pages 188-193, March 10-14, 2008.
- [19] Gunnar Carlsson, Johan Holmqvist, Erik Larsson, Protocol Requirements in an SJTAG/IJTAG Environment, International Test Conference (ITC'07) Santa Clara, CA, USA, October 2007, Lecture 1.3.
- [20] Tobias Dubois, Mohamed Azimane, Erik Larsson, Erik Jan Marinissen, Paul Wielage and Clemens Wouters, Test Quality Analysis and Improvement for an Embedded Asynchronous FIFO, Design, Automation, and Test in Europe Conference (DATE'07) Nice, France April 2007, pages 859-864.
- [21] Anders Larsson, Erik Larsson, Petru Eles, and Zebo Peng, Optimized Integration of Test Compression and Sharing for SOC Testing, Design, Automation, and Test in Europe Conference (DATE'07) Nice, France, April 2007, pages 207-212.
- [22] Anders Larsson, Erik Larsson, Petru Eles, and Zebo Peng, A Heuristic for Concurrent SOC Test Scheduling with Compression and Sharing, IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS'07) Krakow, Poland, April 2007.
- [23] Erik Larsson and Jon Persson, An Architecture for Combined Test Data Compression and Abort-on-Fail Test, Asia and South Pacific Design Automation Conference (ASP-DAC'07), Yokohama, Japan, January 23-26, 2007.
- [24] Erik Larsson, Combined Test Data Compression and Abort-on-Fail Testing, Norchip Conference, Linköping, Sweden, Nov. 2006.
- [25] Soheil Samii, Erik Larsson, Krishnendu Chakrabarty and Zebo Peng, Cycle-accurate Test Power Modeling and Its Application to SOC Test Scheduling, International Test Conference (ITC'06), Santa Clara, CA, USA, October 24-26, 2006.
- [26] Anders Larsson, Erik Larsson, Petru Eles and Zebo Peng, SOC Test Scheduling with Test Set Sharing and Broadcasting, Asian Test

Symposium(ATS'05), Kolkata, India, December 18-21, 2005.

- [27] David Bäckström, Gunnar Carlsson, and Erik Larsson, Remote Boundary-Scan System Test Control for the ATCA Standard, International Test Conference (ITC'05), Austin, Texas, USA, November 8-10, 2005.
- [28] Erik Larsson and Stina Edbom, Combined Test Data Selection and Scheduling for Test Quality Optimization under ATE Memory Depth Constraint, IFIP VLSI-SOC 2005, Perth, Australia, October 17-19.
- [29] Anders Larsson, Erik Larsson, Petru Eles, and Zebo Peng, Optimization of a Bus-based Test Data Transportation Mechanism in System-on-Chip, 8th Euromicro Conference on Digital System Design (DSD'05), Porto, Portugal, August 30th-September 3rd, 2005.
- [30] Urban Ingelsson, Sandeep Goel, Erik Larsson, and Erik Jan Marinissen, Test Scheduling for Modular SOCs in an Abort-on-Fail Environment, European Test Symposium (ETS'05), Tallinn, Estonia on May 22-25, 2005.
- [31] Stina Edbom and Erik Larsson, An Integrated Technique for Test Vector Selection and Test Scheduling under Test Time Constraint, Asian Test Symposium (ATS'04), Kenting, Taiwan, November 2004.

5.4 Workshops

- [32] Jaynarayan Tudu, Virendra Singh, and Erik Larsson, Scan Cells Reordering to Minimize Peak Power during Scan Testing of SoC, Workshop on RTL and High Level Testing (WRTL), Hongkong, China, November, 2009.
- [33] A. Venray, Virendra Singh, and Erik Larsson, An Even-Odd DFD Technique for Scan Chain Diagnosis, Workshop on RTL and High Level Testing (WRTL), Hongkong, China, November, 2009.
- [34] Pramod Subramanyan, Ram Rakesh Jangir, Jaynarayan Tudu, Erik Larsson, and Virendra Singh, Generation of Minimal Leakage Input Vectors with Constrained NBTI Degradation, East-West Design & Test Symposium (EWDTS), Russia, September, 2009.
- [35] Pramod Subramanyan, Virendra Singh, Kewal K. Saluja, and Erik Larsson, Power Efficient Redundant Execution for Chip Multiprocessors, Workshop on Dependable and Secure Nanocomputing, Lisbon, Portugal, June, 2009.
- [36] Dan Adolfosson, Joanna Siew, Erik Larsson, and Erik Jan Marinissen, Deterministic scan-chain diagnosis for intermittent faults, European Test Symposium (ETS 2009), Sevilla, Spain, May, 2009.
- [37] Vinay N. S., Erik Larsson, and Virendra Singh, Thermal Aware Test Scheduling for Stacked Multi-Chip-Modules, DATE 2009 Friday Workshop on 3D Integration - Technology, Architecture, Design, Automation, and Test, Nice, France, April 2009.
- [38] Mikael Väyrynen, Virendra Singh, and Erik Larsson, Fault-Tolerant Average Execution Time Optimization for System-On-Chips, Frontiers of High Performance Embedded Computing, Bangalore, India, January 2009.
- [39] Virendra Singh and Erik Larsson, On Reduction of Capture Power for Modular System-on-Chip Test, IEEE Workshop on RTL and High Level Testing (WRTL'08), Sapporo, Japan, November 2008.
- [40] Anders Larsson, Xin Zhang, Erik Larsson, and Krishnendu Chakrabarty, SOC Test Optimization with Compression-Technique Selection, International Test Conference, San Jose, CA, USA, October, 2008.
- [41] Michael Söderman and Erik Larsson Test Response Compression for Diagnosis in Volume Production, DAC'08 Workshop on Diagnostic Services in Network-on-Chips (DSNOC), Anaheim, CA, USA, June 2008.
- [42] Erik Larsson, Gunnar Carlsson, and Johan Holmqvist Protocol Requirements in an SJTAG/IJTAG Environment, Nordic Test Forum (NTF) Snekkersten, Denmark, November 2007.
- [43] Erik Jan Marinissen, Dan Adolfosson, Erik Larsson, Sandeep Kumar Goel, Improved Scan Chain Diagnosis, 15th NXP IC Test Symposium (NITS'07), Eindhoven, The Netherlands, June 11, 2007.
- [44] Erik Larsson, Mehdi Amirijoo, Daniel Karlsson, Petru Eles, What impacts course evaluation?, 12th Annual Conference on Innovation and Technology in Computer Science Education, Dundee, Scotland, June 25-27, 2007, page 333, ISSN:0097-8418.
- [45] Anders Larsson, Erik Larsson, Petru Eles, and Zebo Peng, Optimized Integration of Test Compression and Sharing for SOC Testing, Swedish System-on-Chip Conference, Gullmarsstrand, Fiskebäckskil, May 14-15, 2007.
- [46] Johan Holmqvist, Gunnar Carlsson, Erik Larsson, Extended STAPL as SJTAG engine, IEEE European Test Symposium, Freiburg, Germany, May, 2007.
- [47] Erik Larsson, Mehdi Amirijoo, Daniel Karlsson, Petru Eles, What impacts course evaluation? 2nd Workshop on Computer Science Education, Linköping, Sweden, April 12, 2007.
- [48] Tobias Dubois, Mohamed Azimane, Erik Larsson, Erik Jan Marinissen, Paul Wielage, and Clemens Wouters, Novel Test and DFT for an Embedded Asynchronous FIFO Memories, The 14-th IEEE International Workshop on Memory Technology, Design, and Testing (MTDT-2006), Grand Formosa Regent Taipei, Taiwan, August 2-4, 2006.
- [49] Tobias Dubois, Mohamed Azimane, Erik Larsson, Erik Jan Marinissen, Paul Wielage, and Clemens Wouters, High-Quality Low-Cost Test and DFT for an Embedded Asynchronous FIFO, Philips Research IC Test Seminar, Eindhoven, The Netherlands, June, 2006.
- [50] Anders Larsson, Erik Larsson, Petru Eles, and Zebo Peng, SOC Test Scheduling with Test Set Sharing and Broadcasting, Swedish System-on-Chip Conference (SSoCC), Kolmården, Sweden, May 4-5, 2006.
- [51] Erik Larsson and Irtiyaz Gilani, A Test Data Compression Architecture with Abort-on Fail Capability, IEEE Workshop on RTL and High Level Testing (WRTL), Harbin, China, July 20-21, 2005.
- [52] David Bäckström, Gunnar Carlsson and Erik Larsson, Boundary-Scan Test Control in the ATCA Standard, IEEE European Board Test Workshop (EBTW), Tallinn, Estonia, May 25-26, 2005.
- [53] Anders Larsson, Erik Larsson, Petru Eles, and Zebo Peng, A Constraint Logic Programming Approach to SOC Test Scheduling, Swedish System-on-Chip Conference (SSoCC), Tammsvik, Sweden, April 18-19, 2005.
- [54] Erik Larsson, SOC Test Design Including Selection of Cores and Tests, Workshop on RTL and High Level Testing (WRTL), Osaka, Japan, November 11-12 2004.