

# TDTS10: Computer Architecture

Lesson  
2017

# Outline

- Lab organization and goals
- SimpleScalar architecture and tools
- Exercises

# Organization

- Assistants
  - Group A, B: [Arian Maghazeh](#)
  - Group C, D: [Rouhollah Mahfouzi](#)
- Web page
  - <http://www.ida.liu.se/~TDTS10>
  - Check the lab page!

# Organization

- [Sign up](#) in Webreg
- Deadline for the assignments:

Lab 1	Nov. 23 <sup>rd</sup>
Lab 2	Dec. 8 <sup>th</sup>
Lab 3	Dec. 19 <sup>th</sup>

- [Rules](#): Read them!

# Lab Schedule

Lab schedule for groups  
A (by Arian) and C (by Rouhollah)

Date	Time	Location	Type
Nov. 7	13:15-15:00	BL34 (Group A) BL33 (Group C)	Lesson
Nov. 7	15:15-17:00	SU04 (Group A) SU17/18 (Group C)	Lab
Nov. 16	08:15-10:00	SU00-01 (Group A) SU17/18 (Group C)	Lab
Nov. 24	15:15-17:00	SU02-03 (Group A) SU00-01 (Group C)	Lab
Dec. 1	15:15-17:00	SU00-01 (Group A) SU02-03 (Group C)	Lab
Dec. 7	08:15-10:00	SU02-03 (Group A) SU00-01 (Group C)	Lab
Dec. 14	13:15-15:00	SU02-03 (Group A) SU17/18 (Group C)	Lab

Lab schedule for groups  
B (by Arian) and D (by Rouhollah)

Date	Time	Location	Type
Nov. 7	13:15-15:00	BL34 (Group B) BL33 (Group D)	Lesson
Nov. 9	08:15-10:00	SU00-01 (Group B) SU17/18 (Group D)	Lab
Nov. 17	15:15-17:00	SU10-11 (Group B) SU17/18 (Group D)	Lab
Nov. 28	10:15-12:00 15:15-17:00	SU10-11 (Group B) SU17/18 (Group D)	Lab
Dec. 5	13:15-15:00	SU04 (Group B) SU02-03 (Group D)	Lab
Dec. 11	10:15-12:00	SU00-01 (Group B) SU02-03 (Group D)	Lab
Dec. 18	10:15-12:00	SU17/18 (Group B) SU10-11 (Group D)	Lab

Please only attend your own lab sessions (6 sessions)

# Examination

For each lab:

1. Demonstrate
  - Must be done during lab sessions
  - Both members must be present during demo
2. Report (by email) to your lab assistant
3. Hand in an empty lab cover **signed** by both members
  - Hand in the cover at a lab session, or put it in the box outside your assistant's office

# Labs

- Three labs:
  1. Cache Memories (2 lab sessions)
  2. Instruction Pipelining (2 lab sessions)
  3. Superscalar Processors (2 lab sessions)

# Goals

- Obtain knowledge about computer organization and architecture
- Insights in various trade-offs involved in the design of a processor
- Become familiar with a set of tools necessary for evaluation of computer architectures



# Environment

- Linux
- Simulations are started from a command line (i.e., terminal)
  - To open a new terminal you can press ctrl+alt+t
- Get yourself familiarized with the terminal
  - Ask Google first
  - Ask your assistant
- Make sure you learn the basic commands (i.e., *cd*, *ls*, *cp*, ...)

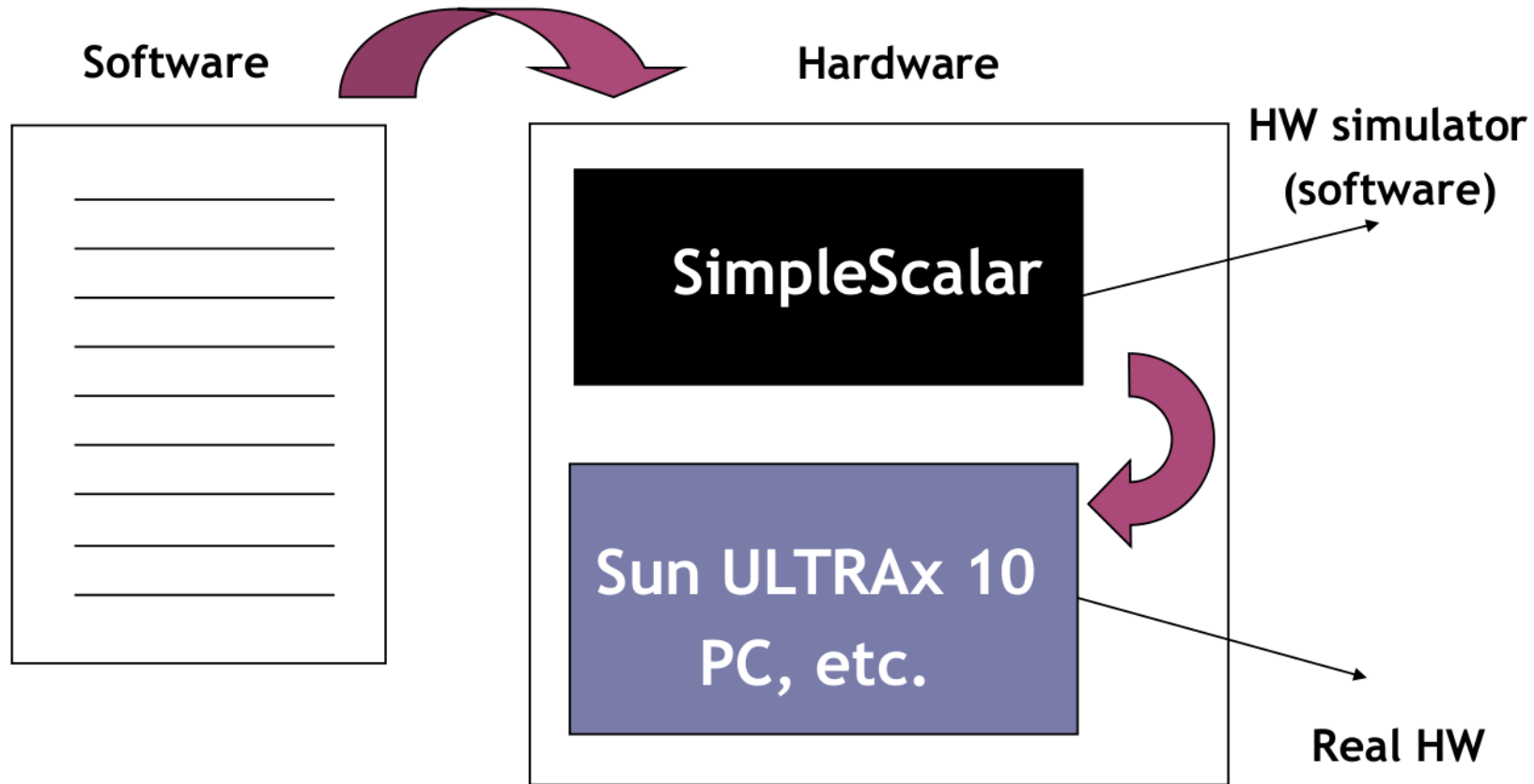
# Tool Setup

- Don't forget the instructions in **lab0**
- Instructions should be clear and easy to follow, but if you face difficulties
  - Don't get frustrated :)
  - Read again carefully (without skipping over the lines)
  - Consult your assistant

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# Architecture Simulation



# SimpleScalar: Literature

- “[The SimpleScalar Tool Set, Version 2.0](#)”, by Doug Burger and Todd M. Austin
  - Very important preparation for the labs
  - This is your main reference for the tool!
- “[User’s and Hacker’s guide](#)”, slides by Austin

# SimpleScalar Architecture

- Virtual architecture derived from MIPS
  - Control (j, jr,..., beq, bne,...)
  - Load/Store (lb, lbu, ...)
  - Integer Arithmetic (add, addu, ...)
  - Floating Point Arithmetic (add.s, add.d, ...)
  - Miscellaneous (nop, syscall, break)

# SimpleScalar Architecture (cont'd)

- Several simulators

- Sim-fast: Fast, only functional simulation (no timing)

- Sim-safe: Sim-fast + memory checks

*Won't use these two!*

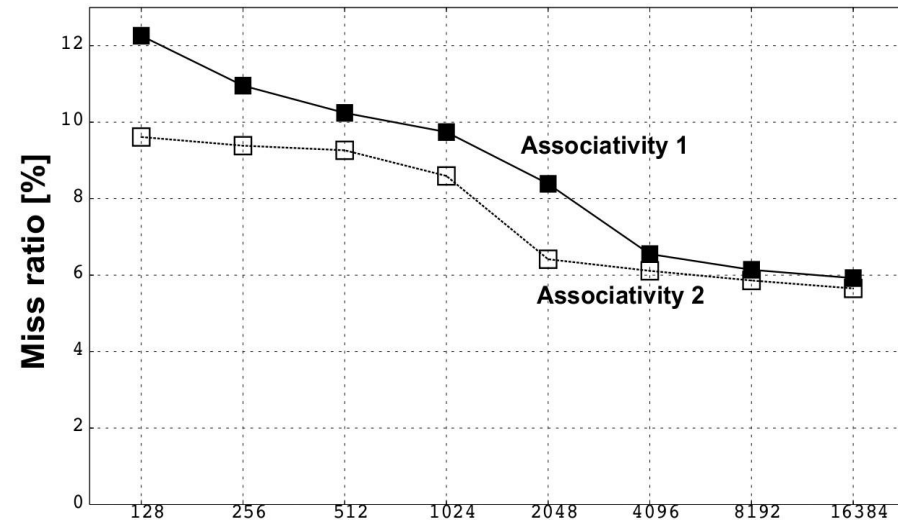
- Sim-cache: Sim-safe + cache simulation and various timing properties (simulation time, measured time, ...)

- Sim-cheetah: Simulation of multiple cache configurations

- Sim-outorder: Superscalar simulator

# An Example

- Lab1, assignment 3
  - Dump the default configuration of sim-cheetah
  - Modify the configuration and simulate
  - Plot the results (e.g. OpenOffice, Gnuplot, Matlab, Excel)





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- **Let's solve some exercises on the first lab!**
  - [Lesson exercises](#)