Note: You can give the answers in English or Swedish.

1. a) Why is memory access the bottleneck of a computer system?

   b) Describe two different methods to increase the bandwidth of the main memory, without using the cache. What are the advantages and disadvantages of the described methods, respectively?

   (3 p)

2. a) Give the definition of seek time, rotational delay, read/write time, and data/transfer rate of a disk memory.

   b) Explain why a hard disk has much better performance in each of the above four measurements, when compared with a floppy diskette.

   (3 p)

3. a) Assume that we have a 4-way set associative cache for a byte-addressable memory. The cache has 128 cache blocks in total and each block consists of 8 bytes. Show how to break the following address into three fields, namely tag, set index, and offset:

   0100 1000 0101 0001 0101 1001

   b) Describe how these three fields are used to locate the content stored in the address in a step by step manner.

   (3 p)

4. Assume that your computer has only 4 GB main memory space, and your friend has just bought a computer game that needs 8 GB memory space to store. Your friend says that you can't run his game on your computer, since it can't even store the game in its main memory. What would you say to your friend? (Hint: You should answer the question of if your computer can run this game or not, and describe the mechanism that is involved in order to justify your answer.)

   (2 p)

5. The following sequence of virtual page numbers is encountered in the course of execution on a computer with virtual memory:

   6 7 6 4 1 3 2 3 6 4 7 1 3 1 5

   Assume that the least-recently used (LRU) page replacement policy is used. Assume also that the main memory has four page frames, and is initially empty. How many page misses will be encountered during this execution? Which are the virtual pages in the main memory when this execution finishes?

   (3 p)

Note: You can give the answers in English or Swedish.

6. a) List all information items that are usually specified in a machine instruction. Describe why each information item is needed.
   b) List and briefly discuss the four main types of machine instructions.

(2 p)

7. a) What does it mean by indirect addressing? Why is it useful to have this addressing mode? What is the disadvantage of using indirect addressing?
   b) Give a concrete example to illustrate how indirect addressing can be used.

(2 p)

8. a) What is a data hazard in an instruction pipeline? Illustrate this hazard by a concrete example and show how penalties are produced (consider a 6-stage pipeline).
   b) Describe an efficient technique to reduce this penalty. Draw figures to illustrate the pipelined executions without and with the described technique.

(3 p)

9. Consider a conditional branch instruction that is executed repetitively with the following outcomes {T, NT, T, NT, ..., T, NT} (i.e., the branch is “taken” every second time, and “not taken” every second time).
   a) What will be the success-prediction rate, if a one-bit predictor is used?
   b) What will be the success-prediction rate, if a bimodal predictor is used? (Note: you can make assumption of the initial state.)
   c) Describe a prediction technique that has a very high success-prediction rate for this type of instructions. Explain why your predictor works well for the considered instruction.

(3 p)

10. a) What does it mean by interrupt-driven I/O? What are the advantages and disadvantages of this technique?
    b) Can the interrupt mechanism be used for other purposes? How? Please give two other examples of using interrupt.

(3 p)

Note: You can give the answers in English or Swedish.

11. a) What is microprogramming? How does it work?

    b) Is the microprogram memory part of the memory hierarchy? Why?

    (3 p)

12. a) Identify all the different types of data dependencies in the following code. Indicate the type of dependency you have identified for each one, and give the reasons for your answers.

```
L1: add r3,r4,#4      Note: r3 := r4 + 4
    store r8,(r3)     Note: memory location pointed by r3 := r8
    sub r8,r5,#4      Note: r8 := r5 - 4
    load r9,(r8)      Note: r9 := memory location pointed by r8
    blt r9,r1,L1      Note: branch to L1 if r9 < r1
```

    b) Are there any dependencies in the above code that can be eliminated? If yes, rewrite the code so that they are eliminated.

    (4 p)

13. a) What are the most essential characteristics of superscalar architecture and VLIW architecture, respectively?

    b) Compare superscalar architecture with VLIW architecture from a performance point of view. Which architecture gives usually better performance? Why?

    (3 p)

14. a) Describe 3 features of RISC computers that you consider as the most important ones for performance improvement. For each feature, describe how it improves the performance of a computer.

    b) Discuss the main differences between the RISC and CISC computers, and the arguments for each of these two different computers.

    (3 p)