

## STATE MACHINES

LECTURE VI TDDI11 Embedded Software

DEPT. COMPUTER AND INFORMATION SCIENCE (IDA) LINKÖPINGS UNIVERSITET

# INTRODUCTORY EXAMPLE: AN ELEVATOR CONTROLLER

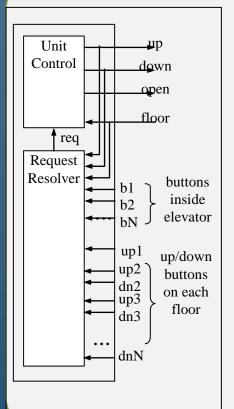
### Simple elevator controller

- Request Resolver resolves various floor requests into single requested floor
- Unit Control moves elevator to this requested floor

#### **Partial English description**

"Move the elevator either up or down to reach the requested floor. Once at the requested floor, open the door for at least 10 seconds, and keep it open until the requested floor changes. Ensure the door is never open while moving. Don't change directions unless there are no higher requests when moving up or no lower requests when moving down..."

#### **System interface**



# ELEVATOR CONTROLLER: A SEQUENTIAL PROGRAM MODEL

#### Sequential program model

Inputs: int floor; bit b1..bN; up1..upN-1;dn2..dnN; Outputs: bit up, down, open; Global variables: int req;

```
void UnitControl()
{
    up = down = 0; open = 1;
    while (1) {
        while (req == floor);
        open = 0;
        if (req > floor) { up = 1;}
        else {down = 1;}
        while (req != floor);
        up = down = 0;
        open = 1;
        delay(10);
    }
}
```

```
void
RequestResolver()
{
  while (1)
  ...
  req = ...
  ...
}

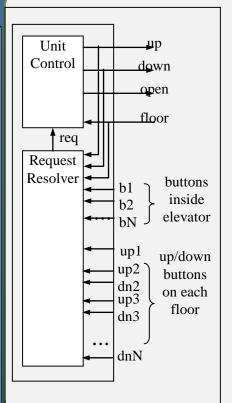
void main()
{
  Call concurrently:
    UnitControl() and
    RequestResolver()
```

#### Partial English description

"Move the elevator either up or down to reach the requested floor. Once at the requested floor, open the door for at least 10 seconds, and keep it open until the requested floor changes.

Ensure the door is never open while moving. Don't change directions unless there are no higher requests when moving up or no lower requests when moving down..."

#### **System interface**



### FINITE-STATE MACHINE (FSM) MODEL

- Trying to capture this behavior as sequential program is a bit awkward
- Instead, we might consider an FSM model, describing the system as:
  - Possible states
    - E.g., Idle, GoingUp, GoingDn, DoorOpen
  - Possible transitions from one state to another based on input
    - E.g., req > floor
  - Actions that occur in each state
    - E.g., In the GoingUp state, u,d,o,t = 1,0,0,0 (up = 1, down, open, and timer\_start = 0)

## STATE MACHINE

- The system is described as a set of states
- Each state is a representation of what the system looks like now and how it got there
- Each state reacts in a specific way to every possible input event, leading to a new state via a transition

# MEALY AND MOORE

- There are two kinds of state machines
  - Mealy and Moore
  - Both are finite state machines
  - Both can capture regular expressions
- Note: Finite state machines and finite automata are used interchangeably

### MOORE MACHINES

A Moore machine is a tuple  $(Q, \Sigma, \Gamma, \Delta, H, q_0)$  consisting in:

- 1. a finite set Q of states where  $q_0$  is the start state
- 2. an alphabet  $\Sigma$  of input letters
- 3. an alphabet  $\Gamma$  of output characters
- 4. a mapping  $\Delta$  associating a state in Q to each pair in  $(Q \times \Sigma)$
- 5. a mapping H associating an output in  $\Gamma$  to each state in Q

$$(q,\sigma) \xrightarrow{\Delta: \text{ transition}} q' \quad \text{where } q,q' \in Q \text{ and } \sigma \in \Sigma$$

$$q \xrightarrow{H: \text{ output}} o \text{ where } q \in Q \text{ and } o \in \Gamma$$

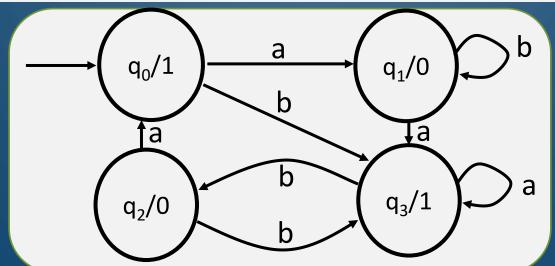
## EXAMPLE OF A MOORE MACHINE

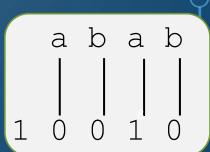
Example: states =  $\{q_0, q_1, \overline{q_2, q_3}\}$ 

 $\Sigma$ ={a,b}

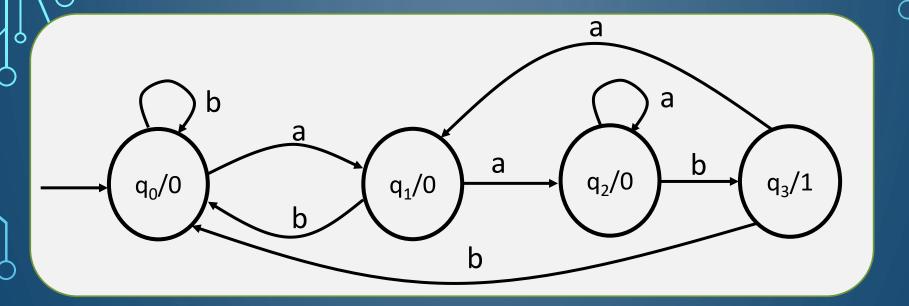
 $\Gamma = \{0,1\}$ 

Old state	Output by the	New state			
	old state	After input a	After input b		
$\rightarrow q_0$	1	$q_1$	$q_3$		
$q_{1}$	0	$q_3$	$q_1$		
$q_2$	0	$q_0$	$q_3$		
$q_3$	1	$q_3$	$q_2$		





# ANOTHER MOORE MACHINE



Input		а	а	а	b	а	b	b	а	а	b	b
State	$q_0$	$q_1$	$q_2$	$q_2$	$q_3$	$q_1$	$q_0$	$q_0$	$q_1$	$q_2$	$q_3$	$q_0$
Output	0	0	0	0	1	0	0	0	0	0	1	0

When does the machine output 1?

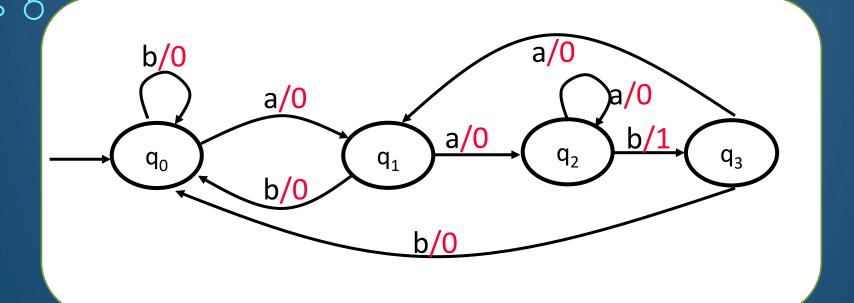
## MEALY MACHINE

A Mealy machine is a tuple  $(Q, \Sigma, \Gamma, \Delta, q_0)$  consisting in:

- a finite set of Q of states where  $q_0$  is the start state
- an alphabet  $\Sigma$  of input letters
- an alphabet  $\Gamma$  of output characters
- a finite set of transitions  $\Delta$  that indicate, for each state and letter of the input alphabet, the state to go to next and the associated output.

$$(q,\sigma)$$
  $\longrightarrow$   $(q',o)$  where  $q,q' \in Q, \sigma \in \Sigma$  and  $\sigma \in \Gamma$ 

# MEALY MACHINE EXAMPLE

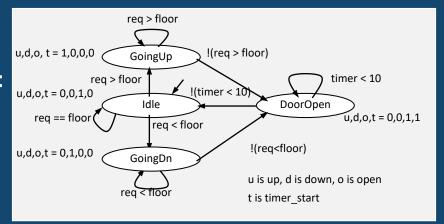


### AN EXTENDED FINITE STATE MACHINE

FSMD extends FSM with Data: complex data types and variables for storing data

An FSMD is a tuple  $(Q, \Sigma, \Gamma, V, \Delta, H, q_0)$ :

- 1. Q is a finite set of states
- 2.  $\Sigma$  is the set of possible inputs
- 3.  $\Gamma$  is the set of possible outputs
- 4. V is a set of variables
- 5.  $\Delta$  associates a state to any triple in  $S \times \Sigma \times V$
- 6. H represents actions: it associates an output and values to V for each state



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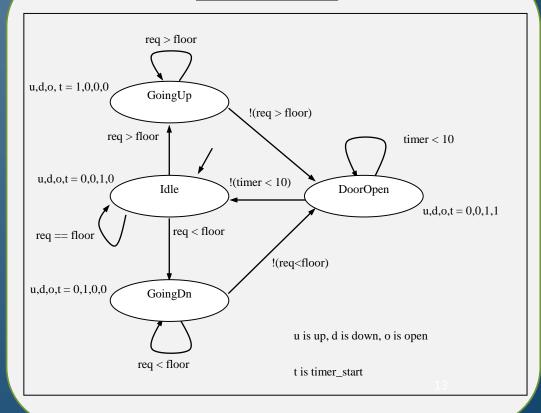
System state completely described by the current state and values of all variables

# DESCRIBING A SYSTEM AS A STATE MACHINE

#### Sequential program model

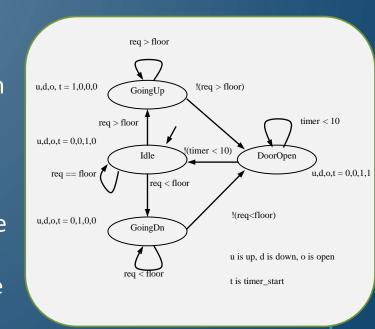
```
Inputs: int floor; bit b1..bN; up1..upN-1; dn2..dnN;
Outputs: bit up, down, open;
Global variables: int req;
void UnitControl()
                                 void RequestResolver()
 up = down = 0; open = 1;
                                   while (1)
 while (1) {
   while (req == floor);
                                     req = ...
   open = 0;
   if (req > floor) \{ up = 1; \}
   else \{down = 1;\}
                                  void main()
   while (req != floor);
   up = down = 0;
                                    Call concurrently:
   open = 1;
                                      UnitControl() and
   delay(10);
                                      RequestResolver()
```

#### **State machine model**



# DESCRIBING A SYSTEM AS A STATE MACHINE

- 1. List all possible states
- 2. Declare all variables
- 3. For each state, list possible transitions, with conditions, to other states
- 4. For each state and/or transition, list associated actions
- 5. For each state, ensure exclusive and complete exiting transition conditions
  - No two exiting conditions can be true at same time. Otherwise nondeterministic state machine
  - One condition must be true at any given time



## STATES AND ACTIONS

States are circles when drawn graphically in a state diagram

- A descriptive name is written within
- An action, what to do as long as staying in this state (which outputs to set, or code to execute) is written next to the circle
- The action should set every output to a known value
- For each possible input event a transition arrow leads out from the state in to some other state

### TRANSITIONS

Transitions are arrows out from one state in to another

- A condition is associated with each arrow
- When the condition is true the transition is performed, the machine moves to the state indicated by the transition
- If none of the transitions from a state is true, the default transition should be to stay in that state

# STATE MACHINE VS. SEQUENTIAL PROGRAM MODEL

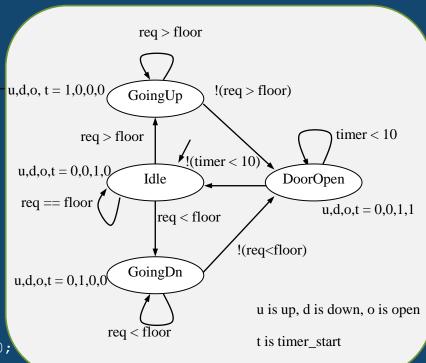
- Different thought process used with each model
- State machine:
  - Encourages designer to think of all possible states and transitions among states based on all possible input conditions
- Sequential program model:
  - Designed to transform data through series of instructions that may be iterated and conditionally executed

# CAPTURING STATE MACHINES IN SEQUENTIAL PROGRAMMING LANGUAGE

- Despite benefits of state machine model, most popular development tools use sequential programming language
  - C, C++, Java, Ada, VHDL, Verilog, etc.
  - Development tools are complex and expensive, therefore not easy to adapt or replace
- Two approaches to capturing state machine model with sequential programming language
  - Front-end tool approach
  - Language subset approach

### LANGUAGE SUBSET APPROACH

```
#define IDLE 0
#define GOINGUP 1
#define GOINGDN 2
#define DOOROPEN 3
void UnitControl() {
   int state = IDLE;
   while (1) {
      switch (state) {
         IDLE: up=0; down=0; open=1; timer start=0;
                  (req==floor) {state = IDLE;}
                 (reg > floor) {state = GOINGUP;}
                 (reg < floor) {state = GOINGDN;}</pre>
            i f
            break;
         GOINGUP: up=1; down=0; open=0; timer start=0;
                 (req > floor) {state = GOINGUP;}
                 (!(reg>floor)) {state = DOOROPEN;}
            i f
            break:
         GOINGDN: up=1; down=0; open=0; timer start=0;
                 (req < floor) {state = GOINGDN;}</pre>
                 (!(req<floor)) {state = DOOROPEN;}
            if
            break:
         DOOROPEN: up=0; down=0; open=1; timer start=1;
            if (timer < 10) {state = DOOROPEN;}</pre>
            if (!(timer<10)) {state = IDLE;}</pre>
            break;
```

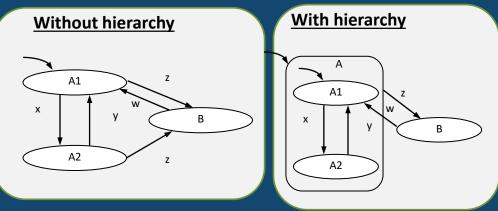


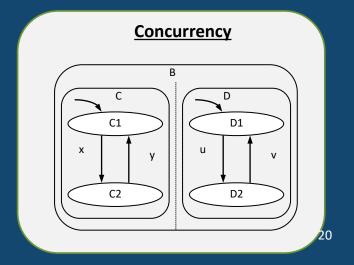
# HIERARCHICAL/CONCURRENT STATE MACHINE MODEL

Another Model for state-based specification

 Uses Hierarchies and Concurrency to eliminate clutter and clarify the structure

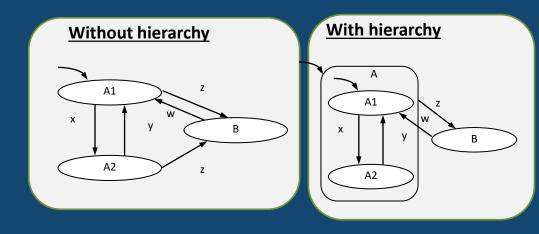
Allows states to be grouped together



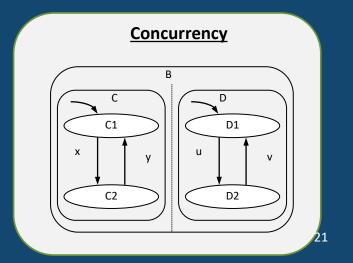


### GROUPS IN STATECHART

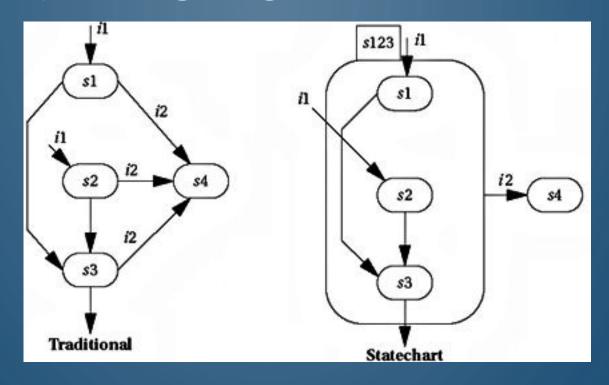
 Statecharts define a language for HCFSMs



- Two groups are
  - OR
  - AND

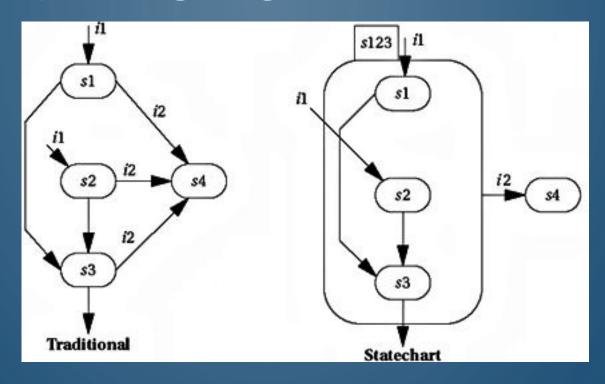


### EXAMPLE OF OR



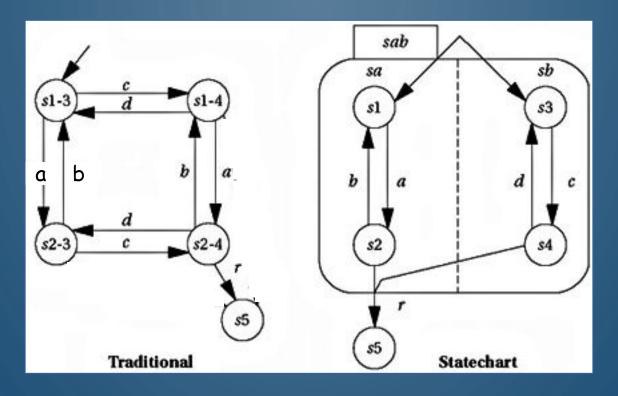
- The machine goes to s4 from s1, s2, s3
- Statechart captures this by having one state around s1, s2, and s3

### EXAMPLE OF OR



- A single transition out of s123 means that on event i2, all states go to s4.
- The OR state allows transitions between its own internal states

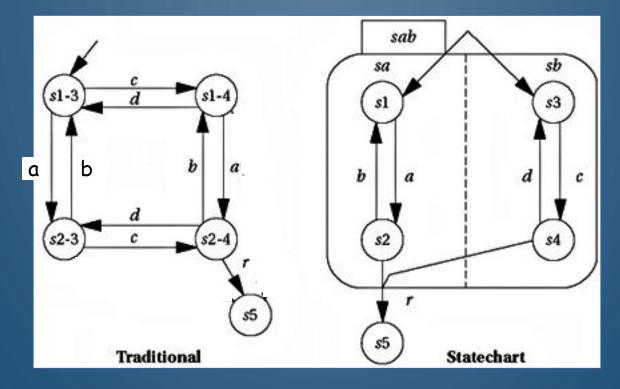
## EXAMPLE OF AND GROUP



The traditional model has many transitions

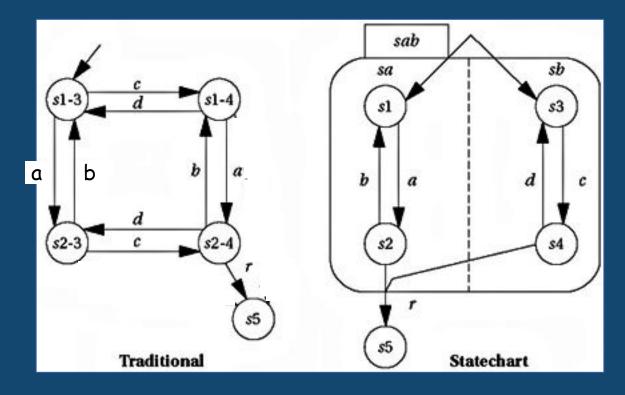
- Between states
- Going out of all states
- One initial transition

## EXAMPLE OF AND



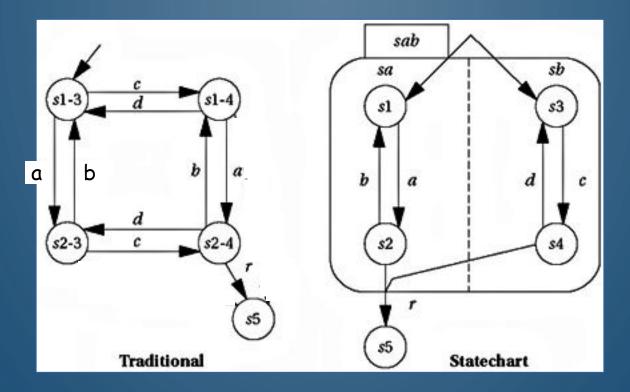
- The statechart has an AND state called sab
- sab has two components sa and sb
- When the machine enters the state sab, it is simultaneously in both sa and sb
  - We must know both sa and sb to know sab

### EXAMPLE OF AND



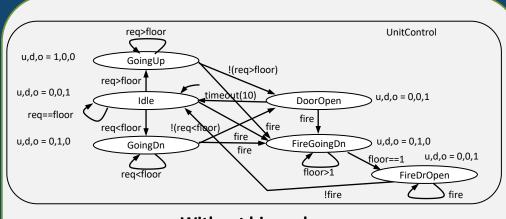
- The name of states reveal their relations
- s1-3 corresponds to sab in s1 and in s3
- When the machine enters the state sab, it is simultaneously in both sa and sb

## EXAMPLE OF AND



 Both models describe the same behavior but the statechart is much simpler, cleaner and easier to understand

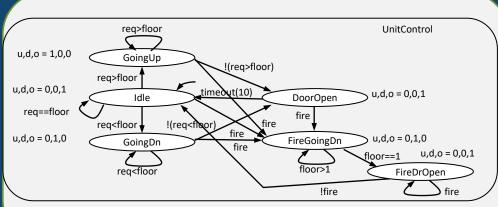
### EXAMPLE OF HCFSM MODELING



Without hierarchy

- FireMode
  - When fire is true, move elevator to 1st floor and open door
    - w/o hierarchy: Getting messy!
    - w/ hierarchy: Simple!

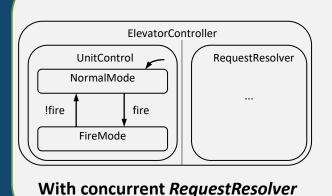
### EXAMPLE OF HCFSM MODELING



- FireMode
  - When fire is true, move elevator to 1st floor and open door
    - w/o hierarchy: Getting messy!
    - w/ hierarchy: Simple!

With hierarchy

#### Without hierarchy



UnitControl NormalMode req>floor u,d,o = 1,0,0GoingUp !(req>floor) rea>floor u,d,o = 0,0,1u.d.o = 0.0.1Idle DoorOpen timeout(10) rea==floo !(req>floor) req<floor u,d,o = 0,1,0!fire GoingDn req<floor FireMode fire u,d,o = 0,1,0FireGoingDn u.d.o = 0.0.1FireDrOpen