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A nonpipelined processor has a clock rate of 2.5 GHz. An upgrade to the processor introduces a five-stage pipeline. However, due to internal pipeline delays, the clock rate of the new processor has to be reduced to 2 GHz.

What is the speedup achieved for a sequence of 100 instructions?



Consider the following assembly language program:

I1:Move R3, R7 $R3 \leftarrow R7$ I2:Load R8, (R3) $R8 \leftarrow (R3)$ I3:Add R3, R3, 4 $R3 \leftarrow R3 + 4$ I4:Load R9, (R3) $R9 \leftarrow (R3)$ I5:BLE R8, R9, L3Branch if R9 > R8

Show the dependencies.



a. Identify the dependencies in the following code:

I1: $R1 \leftarrow R6 + 100$

- I2: $R5 \leftarrow R1 + R2$
- I3: $R7 \leftarrow R5 + 1$
- I4: $R1 \leftarrow R2 + R4$
- I5: $R5 \leftarrow R6 + 22$
- I6: $R2 \leftarrow R4 25$
- I7: $R3 \leftarrow R7 2$
- $18: R4 \leftarrow R1 + R3$
- I9: R10 ← R6 100

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I10: R1 ← R1 + 30
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- b. Rename the registers in the above sequence to prevent, where possible, dependency problems.
- c. Consider a superscalar computer on which the execution of each instruction takes one cycle; the computer has two arithmetic units. Show how instructions are executed in consecutive cycles with: c1) in order execution;
 - c2) out of order execution before renaming;
 - c3) out of order execution after renaming.



An application program is executed on a nine-processor cluster. The program took time *T* on this cluster. Further, it was found that 25% of T was time in which the application was running simultaneously on all nine processors. The remaining time, the application had to run on a single processor.

- a. Calculate the speedup under the aformentioned conditions (relative to execution on a single processor).
- b. Suppose that we are able to effectively use 17 processors rather than 9 on the parallelized portion of the code. Calculate the speedup (relative to execution on a single processor) that is achieved.

