Seminar 2

1. Instruction Pipelining

2. Superscalars

3. Parallel Architectures
Problem 1

A nonpipelined processor has a clock rate of 2.5 GHz and an average CPI (cycles per instruction) of 4. An upgrade to the processor introduces a five-stage pipeline. However, due to internal pipeline delays, the clock rate of the new processor has to be reduced to 2 GHz.

a. What is the speedup achieved for a sequence of 100 instructions?

b. What is the MIPS (millions of instructions per second) rate for each processor?
Problem 2

Consider the following assembly language program:

I1: Move R3, R7 \quad R3 \leftarrow R7
I2: Load R8, (R3) \quad R8 \leftarrow (R3)
I3: Add R3, R3, 4 \quad R3 \leftarrow R3 + 4
I4: Load R9, (R3) \quad R9 \leftarrow (R3)
I5: BLE R8, R9, L3 \quad \text{Branch if } R9 > R8

Show the dependencies.
Problem 3

a. Identify the dependencies in the following code:

I1: \( R1 \leftarrow 100 \)
I2: \( R5 \leftarrow R1 + R2 \)
I3: \( R7 \leftarrow R5 + 1 \)
I4: \( R1 \leftarrow R2 + R4 \)
I5: \( R5 \leftarrow 0 \)
I6: \( R2 \leftarrow R4 - 25 \)
I7: \( R3 \leftarrow R7 - 2 \)
I8: \( R4 \leftarrow R1 + R3 \)
I9: \( R10 \leftarrow 0 \)
I10: \( R1 \leftarrow R1 + 30 \)

b. Rename the registers in the above sequence to prevent, where possible, dependency problems.

c. Consider a superscalar computer on which the execution of each instruction takes one cycle; the computer has two arithmetic units. Show how instructions are executed in consecutive cycles with:

c1) in order execution;
c2) out of order execution before renaming;
c3) out of order execution after renaming.
An application program is executed on a nine-processor cluster. The program took time $T$ on this cluster. Further, it was found that 25% of $T$ was time in which the application was running simultaneously on all nine processors. The remaining time, the application had to run on a single processor.

a. Calculate the speedup under the aforementioned conditions (relative to execution on a single processor).

b. Suppose that we are able to effectively use 17 processors rather than 9 on the parallelized portion of the code. Calculate the speedup (relative to execution on a single processor) that is achieved.
Problem 5

The following program is to be executed on a processor, and a parallel version is to be executed on a 32-processor cluster:

L1: \textbf{for} (i=0; i<1024; i++){
L2: \hspace{1em} sum[i] = 0;
L3: \hspace{1em} \textbf{for} (j=0; j<=i; j++)
L4 \hspace{1em} sum[i] = sum[i]+i
L5 \hspace{1em} }

Suppose lines 2 and 4 each take two machine cycle times, including all processor and memory access activities. Ignore the overhead caused by the software loop control statements (lines 1, 3, 5) and all the system overhead and resource conflicts.

a. What is the total execution time (in machine cycle times) of the program on a single processor?

b. Divide the i-loop iterations among the 32 processors as follows: processor 1 executes the first 32 iterations (i= 0 to 31), processor 2 executes the next 32 iterations, and so on. What are the execution time and speedup factor compared to execution on a single processor.

c. Explain how to modify the parallelizing to facilitate a balanced parallel execution of all the computational workload over 32 processors.

d. What is the minimum execution time resulting from the parallel execution on 32 processors? What is the resulting speedup over a single processor?