

Tentamen i kursen
Datorarkitektur - TDDI 68
2000-04-27, kl. 08-12

Hjälpmedel:

Inga.

Poänggränser:

Maximal poäng är 40.

För godkänt krävs sammanlagt 21 poäng.

Resultat anslås:

Senast 2000-05-11 på IDAs anslagstavla för tentamensresultat.

Jourhavande lärare:

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Good luck !!!

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Du kan skriva på svenska eller engelska!

1. Show a traditional memory hierarchy. What are the parameters according to which the hierarchy is organized.
(3p)
2. *Locality of reference* is an important feature of programs, in the context of memory hierarchies. Explain what *locality of reference* means and why it is important.
(3p)
3. Which are the main characteristics of the following mapping strategies for cache memories: *direct* and *set associative*? Illustrate with a figure for each one.
(4p)
4. What is the purpose of instruction pipelining? How does a pipelined unit work? Illustrate by an example.
(3p)
5. Define the three types of pipeline hazards. Give an example for each.
(2p)
6.
 - a) Why is branch prediction important?
 - b) Illustrate your answer by showing how a certain instruction sequence, of your choice, passes a pipelined unit, in the case of a correct and in that of an incorrect prediction.
(3p)
7.
 - a) What is a superscalar architecture?
 - b) Draw a block-diagram of a superscalar unit.
(3p)

8.

- a) What is the “window of execution” in a superscalar architecture. Why is it important?
- b) Why should the window of execution be large and what are the main problems in this context?

(2p)

9. What is trace scheduling? How does it work (remember the three steps)? Why is it important with VLIW architectures?

(3p)

10.

- a) What is branch predication (like in the Merced/Itanium architecture)? How does it work?
- b) Compare with ordinary branch prediction.

(3p)

11. What is speculative loading with the Merced/Itanium architecture? How does it work?

(3p)

12. What is a vector processor? Draw a block diagram.

(3p)

13. Enumerate at least five factors which limit the achievable speedup that can be obtained using a parallel computer.

(3p)

14. What is the basic idea with the MMX extensions to the INTEL architecture?

(2p)