

Tentamen i kursen Datorarkitektur - TDDI 68, 1999-04-12, kl. 14-18

Du kan skriva på svenska eller engelska!

7.

- a) Describe the strategy for static branch prediction depending on the branch direction.
- b) Describe the strategy for dynamic branch prediction with an one-bit scheme.
- c) Compare how the two approaches work in the case of a loop like the one below:

```
LOOP  -----  
      -----  
      -----  
      BNZ   LOOP  
      -----
```

(4p)

8. The design of RISC architectures is based on certain characteristics of currently used programs. Enumerate at least five such characteristics (Attn! This question is for characteristics of *programs*, not of the RISC processors).

(3p)

9.

- a) Give an example with *output dependency* and another one with *antidependency*. Show how they can be solved by *register renaming*.
- b) Which data dependencies have to be considered by a superscalar CPU using:
 - in-order issue with in-order completion?
 - out-of-order issue with out-of-order completion?

(4p)

10. Flynn's classification of computer architectures: give the definition of the alternative architectures and draw for each one a block diagram.

(3p)

11. What is the role of the mask register in a vector unit?

(2p)

12. We have introduced two features characteristic to parallel computations: f (the ratio of computations that have to be executed sequentially) and f_c (the fractional communication overhead). Discuss how these features influence the performance of parallel architectures and how they have to be considered for determining the number of processors and the size of processes.

(3p)

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1. What is the task of the control unit inside a CPU. Which are the two main techniques for the implementation of control units?.

(3p)

2. *Locality of reference* is an important feature of programs, in the context of memory hierarchies. Explain what *locality of reference* means and why it is important.

(3p)

3. Which are the main characteristics of the following mapping strategies for cache memories: *direct* and *set associative*? Illustrate with a figure for each one.

(4p)

4. What is the role of the translation lookaside buffer (TLB) in a virtual memory system.

(3p)

5. What is a data hazard in a pipelined unit? Illustrate by an example and show how penalties are produced (consider a 6 stages pipeline). How can this penalty be reduced with the *forwarding technique* (draw figures which illustrate the pipelined executions without and with forwarding).

(4p)

6. Consider the following sequence:

SUB R4,R3 R4 $\leftarrow$ R4 - R3

SUB #2,R1 R1 $\leftarrow$ R1 - 2

BEZ TARGET

MOVE R1,R6 R1 $\leftarrow$ R6

TARGET -----

Transform this sequence for a machine with delayed branching.

Show how the original sequence and the transformed one are executed in a six stages pipelined CPU, and illustrate the reduction of the delay (draw a figure which illustrates the corresponding pipelined execution).

(4p)

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Hjälpmedel:

Inga.

Poänggränser:

Maximal poäng är 40.

För godkänt krävs sammanlagt 21 poäng.

Resultat anslås:

Senast 1999-04-26 på IDAs anslagstavla för tentamensresultat.

Jourhavande lärare:

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Good luck !!!