BlueGene/L Design Fundamentals

- Design goals
  - Excellent cost/performance ratio (including operational costs)
  - Good performance/power and performance/volume ratios

- Availability
  - Redundancy, fault detection and fault tolerance
  - Standard proven components for reliability and cost

- Custom advanced components where needed for increased application performance
  - 65 thousands nodes
  - “BG/L Compute” System-on-a-chip
ASIC cost/performance advantage

1. Embedded processor has power/performance advantage
2. System-on-a-chip allows less complexity, denser packaging

BlueGene/L System

- **System**: (64 cabinets, 64x32x32)
- **Cabinet**: (32 Node boards, 8x8x16)
- **Node Board**: (32 chips, 4x4x2)
- **16 Compute Cards**
- **Both processors in a single chip**
- **Compute Card**: (2 chips, 2x1x1)
- **Chip**: (2 processors)
- **2.8/5.6 GF/s 4 MB**
- **5.6/11.2 GF/s 0.5 GB DDR**
- **2.9/5.7 TF/s 16 TB DDR**
- **90/180 GF/s 8 GB DDR**
- **180/360 TF/s 256 GB DDR**
The BlueGene/L Networks

- 3 Dimensional Torus
  - Point-to-point
- Global Tree
  - Global Operations
- Global Barriers and Interrupts
  - Low Latency Barriers and Interrupts
- Gbit Ethernet
  - File I/O and Host Interface
- Control Network
  - Boot, Monitoring and Diagnostics

BlueGene/L Compute ASIC

- IBM CU-11, 0.13 µm
- 11 x 11 mm die size
- 25 x 32 mm CBGA
- 474 pins, 328 signal
- 1.5/2.5 Volt
Dual Node Compute Card

- Heatsinks designed for 15W
- 9 x 512 Mb DRAM; 16B interface
- Metral 4000 connector (180 pins)
- 54 mm (2.125”)
- 206 mm (8.125”) wide, 14 layers

32-way (4x4x2) node card

- 16 compute cards
- Midplane (450 pins) torus, tree, barrier, clock, Ethernet service port
- Ethernet-JTAG FPGA
- 2 optional IO cards
- IO Gb Ethernet connectors through tailstock
- Latching and retention
- dc-dc converters
512 Way BG/L Prototype

Compact Footprint