The purpose of the course is that students shall acquire knowledge on the importance of design of testable digital systems and develop the ability to formulate and solve problems related to testing.

After completing the course, students shall be able to:

- describe fundamental test and fault concepts
- methodically solve test-related problems in a development environment
- formulate and implement test algorithms
- define and implement a minor design-for-test assignment
Recommended Textbook

The recommended textbook is:
- VLSI Test Principles and Architectures,

Additional Literature


Examination

TEN1: Written exam (U,3,4,5), 3 ECTS
- Written examination (max 40 (including 10 points from labs) points)
  - 5=A=34p
  - 4=B=28p
  - 3=C=22p
  - UK=Fx=less than 22p

LAB1: Laboratory work - 3 ECTS
- Can get up to 10 points to include in the written pre-exam”Dugga”.

Laborations

Registration
- The labs should be solved individually. Registration in WebReg.
- Questions regarding the registration are answered by Dimitar
- Last day for the registration is defined by Dimitar

General instructions
- The labs should be handed in using the covers located by the printers
- Last day of handing in the labs will be told by Hans

Instructions and guidelines
- Lab 1 - Test pattern generation
- Lab 2 - Design for test
- Lab 3, 4 - Boundary Scan
Course Outline

- FÖ1: Introduction; Manufacturing, Wafer sort, Final test, Board and System Test, Defects, and Faults
- FÖ2: Test generation; combinational and sequential test generation
- FÖ3: Design-for-Test techniques; test point insertion, scan, enhanced scan
- FÖ4: Built-In Self-Test; Logic BIST and memory BIST
- FÖ5: System Chip Test; test architectures, test planning, test scheduling, and test data compression, power constraints
- FÖ6: System Chip Test; test data compression, test scheduling
- FÖ7: System Test and Boundary Scan
- FÖ8: Diagnosis; scan-chain and logic diagnosis
- FÖ9: Invited speakers
- FÖ10: Study visit (Partnertech, Atvidaberg)

Late Course Registration

- Please find the correct form from: http://www.lith.liu.se/blanketter/
- Fill the form and give it to Patrick Lambrix (director of studies) in office: B 2B:474, Building B, Ground Floor

What is testing?

Design for Test of Digital Systems

TDDC33

Erik Larsson
Department of Computer Science
Making electronic products

Design → Design specification → Production → Product

Types of products:
- First of a kind: product that breaks new ground
- Me too with a twist: improve existing product (example, fast bus)
- Derivate: add a little more functionality
- Next-generation product: replace mature product

Production of electronic products

Wafer → IC → Board → “System”

Products with electronic systems
What is important when purchase?
Power? Performance? Function?
Transistor Count

- Small Scale Integration (SSI), early 1960s
  - Example: Philips TAA320 had two transistors
- Medium Scale Integration (MSI), late 1960s
  - Example: Intel 4004 had 2300 transistors
- Large Scale Integration (LSI), mid-1970s
  - Example: Intel 8008 had 4500 transistors
- Very-Large Scale Integration (VLSI), 1980s
  - Example: Intel 80286, 134000 transistors
- Ultra-Large Scale Integration (ULSI), now
  - More than 1 million transistors

Integrated Circuits (ICs)

- Wafer-scale integration (WSI)
- System-on-a-chip
- Three dimensional integrated circuits (3D-ICs)

IC

- Viper 2.0 RevB
- Analog/Digital TV Processor
- 10mm x 10 mm (100 mm²)
- ~10 M gates
- ~50 M transistors
- ~100 clock domains

Printed Circuit Board (PCB)
Multi-board system

Types of systems

- Analog systems
- Digital systems
- Mixed signal systems

Digital systems

AND-gate
Patterning of SiO2

(a) Silicon base material
(b) After oxidation and deposition of negative photoresist
(c) Stepper exposure
(d) After development and etching of resist, chemical or plasma etch of SiO2
(e) After etching
(f) Final result after removal of resist

Steps in Lithography Process

Lithography has three parts: (1) Light source, (2) Wafer exposure, (3) Resist

Growing the Silicon

Feature size

Linewidth
Space
Thickness
Substrate
Photoresist
Bonding Techniques

- Wire Bonding

Package-to-Board Interconnect

- Flip-chip

IC Defects

- Salt
- Seed

PCB Defects

<table>
<thead>
<tr>
<th>Defect classes</th>
<th>Occurrence frequency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shorts</td>
<td>51</td>
</tr>
<tr>
<td>Opens</td>
<td>1</td>
</tr>
<tr>
<td>Missing components</td>
<td>6</td>
</tr>
<tr>
<td>Wrong components</td>
<td>13</td>
</tr>
<tr>
<td>Reversed components</td>
<td>6</td>
</tr>
<tr>
<td>Bent leads</td>
<td>8</td>
</tr>
<tr>
<td>Analog specifications</td>
<td>5</td>
</tr>
<tr>
<td>Digital logic</td>
<td>5</td>
</tr>
<tr>
<td>Performance (timing)</td>
<td>5</td>
</tr>
</tbody>
</table>

Defects and Faults

- Example of a defect

- A defect manifests itself as a fault
- Fault: permanent or temporary (in respect to time)
  - Permanent (hard)
  - Temporary (soft)

Test

Device under test (DUT)

Stimulus: test vectors
Test pattern: test vector + expected test response (ordered n-tuple of binary values)
Produced test response is compared against expected test response

Important aspects

- Specify the test vector
- Determine correct response (expected response)
- Evaluate quality of test

- Fault coverage = No of faults detected / No. faults modeled
- Defect level (DL) = Number of faulty units shipped / Total number of units shipped.
- Yield = Number of good parts / Total number of tested parts
- Williams and Brown (1981): DL=1-Y^{1-T}
  where Y is yield and T is ratio of covered parts by test.
- For example:
  - If possible to test for all defects: T=1 -> DL=1-Y^{1-T}=0
  - If no defective units manufactured: Y=1 -> DL=1-1^{1-T}=0 (T can be 0)

Feature size

- Shrinking feature size makes it possible to have smaller dies
- Smaller dies makes it possible to have more dies per wafer
- More dies means more chips
- More chips means more money

- BUT, shrinking feature size results in more defect.
- More defect means more dies are defective
- More defective dies means that each wafer gives less chips
- Less chips means less money.

- Which feature size is optimal for overall cost (including test cost)
Diagnosis and volume production

Yield

Diagnosis

First silicon Ramp-up Volume production

Types of Test

- Production
  - Wafer sort (or probe) Test of die on the wafer
  - Final test (package) Test of packaged chips
  - Acceptance Test to demonstrate compliance with purchaser’s requirements
- Sample Test some but not all parts
- Go/No-go Pass or fail test
- Characterization (performance) Test actual parameters
- Stress screening (burn-in) out At high temperature to get wear-out
- Diagnostic (repair) Test to pinpoint defective part
- On-line Test while system is in operation

Making fault free electronic products

Rule of ten: Finding a defect in one later step increases cost with a factor 10 compared to addressing the defect in current step.

Test Preparation Production Test In-Field Test

Manufacturing Test

- Determines whether manufactured chip meets specs
- Must cover high % of modeled faults
- Must minimize test time (to control cost)
- No fault diagnosis
- Tests every device on chip
- Test at speed of application or speed guaranteed by supplier
Burn-in or Stress Test

- **Process:**
  - Subject chips to high temperature & over-voltage supply, while running production tests
- **Catches:**
  - Infant mortality cases – these are damaged chips that will fail in the first 2 days of operation – causes bad devices to actually fail before chips are shipped to customers
  - Freak failures – devices having same failure mechanisms as reliable devices

Types of Test

- Wafer sort - tests the logic of each die on the wafer
- Final test - tests the logic of each packaged IC
- Board test - tests interconnections (soldering errors)

Tests

- Good IC that pass test -> OK
- Bad IC that fail test -> OK
- Bad ICs that pass test -> test escape
- Good ICs that fail test -> yield loss

<table>
<thead>
<tr>
<th>IC</th>
<th>Outcome of test</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Pass</td>
</tr>
<tr>
<td>Good</td>
<td></td>
</tr>
<tr>
<td>Bad</td>
<td>Test esc.</td>
</tr>
</tbody>
</table>

Testing

Automatic Test Equipment (ATE)

- Test stimuli (TS)
- Expected responses (ER)
- Produced responses (PR)
- Compare
- Pass/fail
Automatic Test Equipment Components

- Consists of:
  - Powerful computer
  - Powerful 32-bit Digital Signal Processor (DSP) for analog testing
  - Test Program (written in high-level language) running on the computer
  - Probe Head (actually touches the bare or packaged chip to perform fault detection experiments)
  - Probe Card or Membrane Probe (contains electronics to measure signals on chip pin or pad)

Automatic Test Equipment Companies

- Teradyne was founded in 1960 by two classmates from Massachusetts Institute of Technology (MIT). http://www.teradyne.com/
- LTX was founded in 1976 and the headquarters is in Norwood, MA (Greater Boston), http://www.ltx.com/
- Agilent Technologies (formed in 1999 from a division of Hewlett-Packard), www.agilent.com
- Verigy was in 2006 formed from a division of Agilent Technologies, https://www.verigy.com/

Automatic Test Equipment Companies


Sapphire from Credence
V93000 from Verigy
T6577 from Advantest
Tiger from Teradyne
**Test generation**

Example: Create test for output connected to $V_{dd}$

<table>
<thead>
<tr>
<th>Fault-free</th>
<th>Faulty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1 &amp; 1</td>
<td>1 1 &amp; 1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fault-free</th>
<th>Faulty</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0 &amp; 0</td>
<td>1 1 &amp; 1</td>
</tr>
</tbody>
</table>

**Fault models**

- Stuck-at Fault, Bridging Fault, Shorts (Resistive shorts), Opens, Delay Faults, Transient Fault
- So far stuck-at fault model is the most used one:
  - Motivations:
    - Simple
    - Covers quite well possible defects
  - Above 65 nm: SA0 and SA1
  - At 65 nm -> TMSC standard: 6 fault types; DC-SA0/SA1, AC-input slow to rise (ISR), input slow to fall (ISF), output slow to rise (OSR), output slow to fall (OSF)
  - Below 65 nm (i.e 45 nm and 32 nm): ??

**Test generation**

Example: Create test for output connected to $V_{dd}$

Find test stimuli such that test responses are different in fault-free and faulty device
Stuck-at Fault

- A line is fixed to logic value 0 (stuck-at-0) or 1 (stuck-at-1)
- For the stuck-at fault model there are for a circuit with n lines 2*n possible fault sites
- Quality of a test is given by: fault coverage = faults detected / total number of faults
- Example: 10 lines (20 faults) detect 12 faults: f.c.=12/20 (60%)

Verification, test and diagnosis

- **Verification** is to verify the correctness of the design. It is performed through simulation, hardware emulation, or formal methods. It is performed once prior to manufacturing. Responsible for quality of design.
- **Test** verifies the correctness of manufactured hardware. Test is a two-part process:
  - Test generation: software process executed once during design, and
  - Test application: electrical tests applied to hardware. Test application performed on every manufactured device. Responsible for quality of devices.
- **Diagnosis**: Identification of a specific fault that is present on DUT.

Single Stuck-at Fault

- Three properties define a single stuck-at fault
  - Only one line is faulty
  - The faulty line is permanently set to 0 or 1
  - The fault can be at an input or output of a gate
- Example: XOR circuit has 12 fault sites (●) and 24 single stuck-at faults
- Example: XOR circuit has 12 fault sites (●) and 24 single stuck-at faults

Test vector for h s-a-0 fault