**ASIC** - Application Specific Integrated Circuit

**AC-scan** - sample (capture) is applied at-speed (see also At-speed scan and DC-scan)

**Aliasing**

**APG** - automatic pattern generation, see ATPG

**ATE** - automatic test equipment

**ATPG** - automatic test pattern generation

**At-speed scan** - shift and sample (capture) are applied at-speed

**BILBO** - Built- In Logic Block Observer

**BIST** - built-in self-test

**Boundary Scan** see IEEE 1149.1

**BSDL** - Boundary Scan Description Language

**CUT** - circuit-under-test (see DUT)

**DC-scan** - shift and sample (capture) are applied below normal speed

**Defect level** - fraction of shipped devices that can be expected to be defective (ie. escapes) due to incomplete test coverage. Usually expressed as a percentage number. See DPM.

**DFT** - Design for Testability

**DPM** - defect per million. The defect level expressed as defective parts per million units.

**DUT** - device-under-test (see CUT)

**Fault(s)** - This term is used in reference to classes, or concepts, of defect types. The most common of these is the stuck at type, or fault class. A fault is a software model of a defect, or class of defects.

**Fault coverage**: Quality measure for a test or set of tests, based on the percentage of actually detected faults (defects) versus the total number of theoretically detectable faults, on a particular fault model. A coverage figure should be given for each model type tested. As the operator defines the nodes to be evaluated (in some cases this is done by defining lists of nodes not to be used in the task) the raw number has little meaning without a full analysis of the set up.

**Full scan**: Scan architecture (implementation) where all of the memory elements (flip-flops) are scannable in the design.

**Functional testing**: Also known as behavioral testing. Strategy of testing integrated circuits that focuses on the expected functionality of the circuit. Defects are targeted in an indirect way.
**IEEE 1149.1** IEEE Standard 1149.11990 “Test Access Port and Boundary Scan Architecture” (see www.ieee.org)

**IDDQ**: Quiescent Supply Current (IDD). Theoretically, static CMOS logic should have nearly zero current when the clock is stopped. This methodology puts the chip into various logic states.

**JTAG**: Joint Test Action Group. Originally the name of the team, however, the term has come to be associated with the output of the team. JTAG is now essentially synonymous with the IEEE 1149.1 standard for Test Access Port and Boundary Scan.

**LBIST**: Logic Built In Self Test. A form of BIST targeted at testing random logic. Typically, this is done with PRPGs feeding scan logic and the outputs are connected to a MISRs. All commercial forms of LBIST require a full scan infrastructure.

**LFSR**: Linear Feedback Shift Register. LFSRs are shift registers with exclusive-OR gates that allow some bits in the register (usually referred to as a polynomial) to feed back into selected points within the register. LFSRs are often used in BISTed designs to form PRPGs and MISRs.

**LSSD**: Level Sensitive Scan Design. Type of scan design that uses master/slave latches which have different clock phases to isolate each scan node.

**MBIST**: Memory Built In Self Test. BIST approach that is specific to memory testing.

**MISR**: Multiple Input Shift Register. Also known as Multiple Input Signature Register. MISRs are simply LFSRs configured as signature analyzers. MISRs are often used on the back end of BIST engines to capture and compress output sequences from a circuit under test.

**Mux-D**: Type of scan design that uses D type flip-flops with input multiplexers to isolate each scan node. This is the most widely used type of scan element.

**Output isolation**: Any mechanism for isolating a core's outputs from the surrounding circuitry, such that the surrounding circuitry may be tested without contention from the cores not under test.

**IEEE 1500**: IEEE standard for test wrappers (common -scan like test structures "wrapped around SOC cores).

**Parallel Test**: Testing more than one device simultaneously. By convention, this is usually assumed to be identical tests on identical devices. (contrast to Concurrent Test).

**Partial Scan**: Scan architecture (implementation) where only some of the storage elements (flip-flops) are scannable.

**Path Delay**: Fault characterized by a particular logic path being too slow to meet the overall timing requirements of a circuit.

**PI**: Primary Input: Physical input from the outside world to a device, can be a signal input, a scan chain input, etc. (Note: In the case of cores in an SOC, the outside...
PO - Primary Output: Physical output to the outside world from a device, can be a signal output, a scan chain output, etc. (Note: In the case of cores in an SOC, the outside world may still be inside the chip)

PRPG - Pseudo-Random Pattern Generator. PRPGs are LFSRs that are sometimes used on the front end of BIST engines to generate pseudo-random patterns to be presented to a circuit under test.

Scan: DFT technique where traditional functional logic is reconfigured into "chains" for direct test access to internal nodes.

Scan Chain:
Serial organization of scan elements such that the first element of the chain is at a device input and the last element of the chain is at a device output. Devices may use single or multiple scan chains to 'capture' all of the scannable nodes.

Site: When discussing parallel test, a site refers to the logical partitioning of tester resources for each device. When discussing a fault, or defect, the physical location on the chip where the fault or defect lies.

SOC - System on a Chip. Practice of integrating one or more processor cores, embedded memories, peripheral interfaces, and sometimes mixed signal circuits onto a single chip to form a complete (or nearly complete) system.

SRSG - Shift Register Sequence Generator. A simple PRPG (single output) - defined here because it's used in the definition of STUMPS.

STDF - Standard Test Data Format. STDF is a standard output format for test results. There are numerous tools for post processing STDF generated files and performing statistical analysis on a population of tested devices.

STIL - Standard Test Interface Language. STIL is a standard for test development. It is supported as an output format by the ATPGs of most EDA toolsets. None of the ATEs currently support STIL directly, however because STIL is richer in capabilities than WGL, the industry trend is toward full STIL support. Some testers may eventually support STIL as their native test language.

Structural Testing: Strategy of testing integrated circuits that focuses on detecting manufacturing defects. Unlike functional or behavioral testing, defects are targeted directly.

STUMPS - Self Test Using MISR and Parallel SRSG. STUMPS is a common BIST architecture that combines a PRPG (or multiple SRSGs), multiple scan chains, and a MISR.

TAP - Test Access Port. Part of the JTAG standard, the TAP is a 4 (or optionally 5) pin port to enable boundary scan (see IEEE 1149.1).
TCK - Test Clock (TAP Signal) (see IEEE 1149.1)

TDI - Test Data Input (TAP signal) (see IEEE 1149.1)

TDO - Test Data Output (TAP Signal) (see IEEE 1149.1)

TMS - Test Mode Select (TAP Signal) (see IEEE 1149.1)

Test protocol: A sequence of control operations required to perform a test. At the lowest level a test protocol is just a series of logic 0 and 1 applied to specified test control ports. It will typically also contain symbolic references to the test data that is to be applied to or observed at specified test data or system data ports. Test protocols involve the activation of one or more test modes and may also contain pre-conditioning and post-conditioning functions or sequences.

Transition Delay: Fault characterized by a particular gate or gate connection being too slow-to-rise or too slow-to-fall to meet the overall timing requirements of a circuit.

UDL - User Defined Logic. Special purpose logic added by the SOC chip integrator (e.g. not a purchased IP), for use as "glue" logic, or part of the system chip product differentiator.

Validation: A "post-silicon" process to prove (with evidence) a design to be valid. For our purposes, validation is any use of special purpose test hardware to prove the product meets the design intent; as opposed to other usage of the same equipment as a manufacturing screen.

Verification: A "pre-silicon" process done during development, for gaining confidence, that a Design will produce a pre-defined result. An output of verification may be translated into ATE vectors (used for functional testing).

Wrap I/O: DFT technique where a pin's output is wrapped back in to it's input (or the input of another pin). This can allow some testing of pins that are not contacted directly by the tester. Note: This definition actually does the concept a disservice, because Wrap I/O is really much, much more - though beyond the scope of this glossary.