TDDC33
Design for Test of Digital Systems
Lesson 1

Introduction to the lab series

Dimitar Nikolov, IDA/SaS ESLAB
Outline

- Organization

- Lab Assignments
  - Lab1: Test pattern generation
  - Lab2: Design For Test
  - Lab3: Board testing using Boundary Scan
  - Lab4: Boundary Scan in Action

- Preliminary exams

- Tools
  - Leonardo Spectrum
  - FlexTest
  - DFTAdvisor
  - Trainer1149
  - TSTAP- Studio
Organization

Contact information

- Dimitar Nikolov
- E-mail: dimitar.nikolov@liu.se * start subject line with TDDC33
- Homepage: http://www.ida.liu.se/~dimni
- Office: B 3D:437
Organization

- Course homepage:
  - http://www.ida.liu.se/~TDDC33/

- Lab web-pages:

- Register in WebReg
  - https://www.ida.liu.se/webreg/TDDC33-2011/REGISTRATION

- The labs are mandatory part of the course and have to be solved individually
Organization

Important dates:

- Registration deadline: 2011-09-12
- Deadlines for submitting lab reports:
  - LAB 1: Monday 19th September 2011.
  - LAB 2: Monday 03rd October 2011.
  - LAB 3: Monday 17th October 2011.
  - LAB 4: *requires no lab report
- Updates to returned lab reports must be handed in within 7 days after receiving the notification emails

- Preliminary exams (dugga)
  - Preliminary exam I : Monday 19th September 2011
  - Preliminary exam II : Monday 03rd October 2011
Organization

What do you get for doing the labs?

- All points you gain will be counted into your mark of the final examination
- **0-5 points** for each preliminary exam (DUGGA)
- Up to **10 points** for doing the labs (5 from each preliminary exam)
- Up to **40 points** for the final exam  
  (30 points for written exam + 10 points for labs)
Organization

- Examination of labs
  - Preliminary exam ("dugga") ~20 minutes
  - Oral presentation (prepare to answer questions and to show that you can handle the tools)
  - Written report (one for each lab*) containing the results from the lab.
  - Use the Laboration report covers found in the printing rooms.

- Personal experience of the lab. Not graded. Comments on:
  - level of difficulty,
  - instructions, tools, effort and time, etc.

*Lab 4 does not require a written report
## Organization

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  - Trainer1149
  - TSTAP- Studio
Lab 1: Test Pattern Generation

- **Objective**
  - To get experience and knowledge about test pattern generation for combinatorial and sequential circuits.

- **Input**
  - Two designs c17 and s27 described in VHDL

- **Assignment 1: Manual test pattern generation**
  - Number of test patterns used
  - Achieved fault coverage
  - Test patterns

- **Assignment 2: Automatic test pattern generation**
Lab 1: Test Pattern Generation

- **Challenging task:**
  - Try to achieve high fault coverage with minimal set of test patterns
  - The results will be published on the course web-page

- **Lab Report expectations:**
  - Report the manually generated test patterns
  - Report the achieved fault coverage
  - Report the fault coverage when using the patterns obtained by the Automatic Test Pattern Generation
Lab 2: Design For Test

- Objective
  - To get experience and knowledge about different design for test techniques.

- Input
  - One sequential design s27 described in VHDL

- Assignment 1: Manual test point insertion
  - Number of test points added
  - Achieved fault coverage before adding test points
  - Achieved fault coverage after adding test points

- Assignment 2: Automatic scan chain insertion
Lab 2: Design For Test

- **Lab Report Expectations:**

<table>
<thead>
<tr>
<th></th>
<th>No DFT</th>
<th>Manual Test Point Insertion</th>
<th>Full-Scan</th>
<th>Partial-Scan</th>
<th>Partial-Scan + Manual Test Point Insertion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Report Fault Coverage</td>
<td>Report Fault Coverage + number of test points used</td>
<td>Report Fault Coverage</td>
<td>Report Fault Coverage + number of Scan Cell used</td>
<td>Report Fault Coverage + number of test points used</td>
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- **Discuss the results**
Lab 3: Board testing using Boundary Scan

- **Objective**
  - To get experience and knowledge about board testing using boundary scan.

- **Input**
  - A board design called TDDC33 consists of two chips, c17 and s27.

- **Assignment 1: Design modification for Boundary Scan**
  - Draw a new design of the board where the Boundary Scan interface (TDI, TDO, TMS, and TCK) is added

- **Assignment 2: Interconnect test**
  - Write an interconnect program that detects at least one fault for each of the following four types of faults: Stuck-at 1, Stuck-at 0, Wired-AND short, and Wired-OR short
  - Verify the test program by introducing faults in the design.
Lab 4: Boundary Scan in action

- Assignment 1: Improving Boundary Scan fault coverage
  - Create a project in TSTAP-Studio, generate test patterns, by using TSTAP’s pattern generation tool, modify the nodelist file in order to obtain better fault coverage. Run the tests generated from the TSTAP-PG pattern generation tool. Remember the boards have already been tested, and it is verified that the boards are working properly.

- Assignment 2: Tests for diagnosing potential faults on the board
  - Inject faults on the board
  - Use the TSTAP-RT tool to run different types of tests on the connected demo board. For the erroneous tests try to discover what may be the error.
Lab 4: Boundary Scan in action

SAAB

TSTAP-Studio
Scanway-USB Controller
Demo Board

Lab Assignments
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Preliminary exams

- Two preliminary exams

- Preliminary exam I will cover test pattern generation and design for testability techniques

- Preliminary exam II will cover 1149.1 JTAG specification and Boundary scan testing

- From each exam you can get up to 5 points which will be added to the overall mark
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Leonardo Spectrum

- Used to synthesize a compiled design, described in VHDL, to a netlist (Verilog format)
- A cell core library is used as an external source in the synthesis process
- The netlist is the output of the synthesis process. It contains information about which cells are used and how they are connected among each other.
DFTAdvisor

- Used to insert scan-chains in the design
- Scan-chain is one of the techniques which is widely used in Design For Testability (DFT)
- The tool uses a Verilog netlist as input, and modifies it by inserting scan-chains.
- Cell core library is required
- Enables you to choose which kind of Scan architecture to use, either a Full-Scan design, or Partial-Scan design
FlexTest

- Used for fault-simulation and test pattern generation
- Uses a Verilog netlist as input
- Gives you information about the fault-coverage and generates test patterns
Flow of using Mentor Graphics’ tools

Start

Leonardo Spectrum

Insert Scan Chains

Yes

DFTAdvisor

Yes

FlexTest

Yes

Improve FC by using other test patterns

No

Improve FC by inserting Scan Chains

No

Improve FC by inserting test points

No

End
Trainer 1149

- Used for Boundary Scan
- Performs interconnect tests
- Allows fault injection
- Helps understanding Boundary Scan
TSTAP-Studio

- Used for Board Testing
- Perform Boundary Scan tests
- Applicable for In-System Programming
- Applicable for Flash Programming
- Creating tests in BSL (Boundary scan Stimuli Language)
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Lesson 1

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