Exam/Tentamen

TDDC33 Design for Test of Digital Systems

/Design av digitala testbara system/

2007-11-22, kl. 14-18

Sal
Kårallen

Resultat anslås:
Senast 2008-01-04

Jour:
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Admitted material
Dictionary from English to your native language;

General instructions
This exam has 7 assignments and 3 pages, including this one.
Read all assignments carefully and completely before you begin.

- It is recommended that you use a new sheet for each assignment. Number all your sheets, and mark each sheet on top with your name, personnummer, and the course code.
- You may answer in English or Swedish.
- Write clearly. Unreadable text will be ignored.
- Be precise in your statements. Imprecise formulations may lead to a reduction of points.
- Motivate clearly all statements and reasoning.
- Explain calculations and solution procedures.
- The assignments are not ordered according to difficulty.
- The exam is designed for 30 points. You may thus plan about 8 minutes per point.
- Grading: U, 3, 4, 5. The preliminary threshold for grade 3 is 20 points.

Good luck
1) Test generation (10 points)
(a) Motivate if/iff not the test vector a=1, b=1, c=0 is a test for stuck-at-0 on the highlighted line in the circuit (2p):

(b) List two test generation algorithms (2p).
(c) In order to provoke a SA1 fault, would you insert a D or a D’ (motivate) (2p).
(d) In order to ensure that a D propagates from one input of a two-input AND to the output, what should the other input be set to (2p)?
(e) Fault equivalence reduces the number of fault sites. How many equivalent fault sites under the stuck-at fault assumption exists for a two-input AND gate (2p)?

2) Design for Test (4 points)
(a) List and motivate two advantages with scan-chains (1p).
(b) List and motivate two disadvantages with scan-chains (1p).
(c) What is the test time for applying 5 test patterns to an ASIC with 10 scan-flip flops, which are formed as a single scan-chain (1p)?
(d) What is the lowest possible test time for a core with 5 test patterns and where the scan-chains are formed into two wrapper-chains where the number of scan flip-flops is 10 and 15, respectively (1p)?

3) Built-In Self-Test (6 points)
(a) What is the complexity of the following MARCH algorithm: \{ \uparrow(w_0, r_0), \downarrow(w, r_0), \uparrow(w_0, r_0, w_1, r_1, r_0) \}(1p)?
(b) What should the memory contain (in a fault-free case) after applying the memory test algorithm above (1p)?
(c) Assume a STUMPS architecture and an LFSR as below. The LFSR output a is connected to circuit input a. Given the initial seed of 000 in the LFSR, which are the three first patterns and which faults do they detect (4p)?
4) System-on-Chip Test (4 points)
a) For a system with so called hard cores, the number of wrapper-chains are fixed, compare (show the test time and draw a figure of the test schedule) the testing times for Multiplexing test architecture and Distribution test architecture for an SOC with 4 cores, A, B, C, and D. The testing times for core A, B, C, and D is 5, 10, 10, 20, respectively and number of wrapper chains per core, A, B, C, and D, is 4, 4, 2, 4. The ATE has 10 channels (2p).
b) What is the shorties shift in time/shift out time in clock cycles for a IEEE 1500 wrapped core that has 4 inputs, 2 outputs and 2 scan-chains of length 10 and 12 (2p)?

5) Test Data Compression(2 points)
a) List differences between Logic BIST and test data compression (discuss test source and test sink) (2p)?

6) Diagnosis (2 points)
a) Assume that the output pattern from a so called flush test is as follows: \{111111\}. What is the fault type? At which flip-flop is the fault? (2p)

7) Board Test (2 points)
a) How many additional pins are required in order to employ Boundary Scan (IEEE 1149.1) (1p.)
b) Is INTEST a mandatory instruction in IEEE 1149.1: why/why not (1 p.)?