

STRINGENT 1st half of 2003

Journals

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3. E Elias, P Löwenborg, H Johansson, L Wanhammar: "Tree-structured IRR/FIR uniform-band and octave-band filter banks with very low-complexity analysis or synthesis filters", to appear in *EURASIP Sign. Proc.*
4. O. Gustafsson, H Johansson, L Wanhammar: "Single filter frequency masking high-speed recursive digital filters", *Circuits, Syst., Signal Processing*, vol 22, No 2, pp 219-238, 2003.
5. S Hsu, A Alvandpour, S Mathew, S Lu, R Krishnamurthy, S Borkar: "A 4.5 GHz 130nm 32-kb LO cache with a leakage-tolerant self reverse-bias bitline scheme", *IEEE Journal of Solid-State Circuits*, Vol 38, No. 5, May, pp 755-761, 2003.
6. H Johansson: "Multirate IRR filter structures for arbitrary bandwidths", accepted for publication in *IEEE Trans. Circuits Syst. I*.
7. H Johansson, P Löwenborg: "On the design of adjustable fractional delay FIR filters", *IEEE Trans Circuits Syst. II*, vol 50, No 4, pp 164-169, April 2003.
8. H Johansson, T Saramäki: "Two-channel FIR filter banks utilizing the frequency-response masking approach", *Circuits, Syst., Signal Processing*, vol 22, No 2, pp 157-192, 2003.
9. R. Jonsson, Q. Wahab, S. Rudner and C. Svensson, "Computational load pull simulations of SiC microwave power transistors", *Solid-State Electronics*, vol. 47, pp. 1921-1926, 2003.
10. E Larsson, K Arvidsson, H Fujiwara, Z Peng: "Efficient test solutions for core-based design", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*.
11. P Löwenborg, H Johansson, L Wanhammar: "Two-channel digital and hybrid analog/digital multirate filter banks with very low complexity analysis or synthesis filters", *IEEE Trans. Circuits Sys II*, Vol 50, No. 7, pp 355-367, July 2003.
12. P Pop, P Eles, Z Peng: "Schedulability analysis and optimization for the synthesis of multi-cluster distributed embedded systems", *IEE Proceedings - Computer & Digital Techniques*, (accepted for publication).
13. T Saramäki, J Yli-Kaakinen, H Johansson: "Optimization of frequency-response-masking base FIR filters", accepted for publication in *J. Circuits, Syst. Comput.*
14. I Söderquist: "Globally updated mesochronous design style", *IEEE Journal of Solid State Circuits*, vol 38, No. 7, pp 1242-1249, July, 2003.

Conferences

1. A Alvandpour, R Krishnamurthy, D Eckerbert, S Apperson, B Bloechel, S Borkar: "A 3.5 GHz 32mW 150nm multiphase clock generator for high-performance microprocessors", *IEEE Int. solid-state circuits conference*, pp 112-113, Feb 9, 2003.
2. A Alvandpour, D Somasekhar, R Krishnamurthy, V De, S Borkar, C Svensson: "Bitline leakage equalization for sub-100nm caches" to be presented at *ESSCIRC*, Estoril, Portugal, Nov 16-18, 2003.
3. KO Andersson, NU Andersson, M Vesterbacka, JJ Wikner: "A method of segmenting digital-to-analog converters", *Proc. IEEE Southwest symposium on mixed-signal design*, Las Vegas, USA, pp 32-37, Feb 23-25, 2003.

4. KO Andersson, NU Andersson, M Vesterbacka, JJ Wikner: "A 14-bit dual current-steering DAC". Proc SSoCC '03, Eskilstuna, Sweden, April 8-9, 2003.
5. S Andersson, C Svensson, O Drugge: "Wideband LNA for a multistandard wireless receiver in 0.18 μm CMOS", ESSCIRC '2003, Estoril, Portugal, Sept 16-18, 2003.
6. E Backenius, M Vesterbacka: "Characteristics of a differential D flip-flop", Proc SSoCC '03, Eskilstuna, Sweden, April 8-9, 2003.
7. H Bengtsson, C Svensson: "Speed study of a 2.5 Gb/s equalizer for optical communication in a 3 V 0.35 μm CMOS process", Proc SSoCC '03, Eskilstuna, April 8-9, 2003.
8. J Carlsson, W Li, K Palmkvist, L Wanhammar, S Zhuang: "A design path for design of GAL based communication systems", Proc. Swedish system-on-chip conference, Eskilstuna, Sweden, April 8-9, 2003.
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11. AG Dempster, O Gustafsson, JO Coleman: "Towards an algorithm for matrix multiplier blocks", Proc European conference circuit theory design, Krakow, Poland, Sept 2003. (accepted conference publication).
12. H Eriksson, T Henriksson, P Larsson-Edefors, C Svensson: "Full-custom vs. standard-cell design flow - An adder case study", Proc of Asia South Pacific design automation conference, Kitakyushu, Japan, pp 507-510, Jan 2003.
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20. E Hjalmarson, R Hägglund, L Wanhammar: "Optimization-based design space exploration on analog circuits", Proc European conference on circuit theory and design, Krakow, Poland, Sept 2003.
21. S Hsu, B Chatterjee, M Sachdev, A Alvandpour, R Krishnamurthy, S Borkar: "A 90nm 6.5 GHz 256x64b dual supply register file with split decoder scheme", Int symposium on VLSI circuits, pp 237-238, 2003.
22. R Hägglund, E Hjalmarson, L Wanhammar: „Using optimization to find design trade-offs in analog amplifier design", Proc of SSoCC '03, Eskilstuna, Sweden, April 8-9, 2003.
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25. D Jakonis, K Folkesson, J Dabrowski, C Svensson: "Downconversion sampling mixer for wideband low-IF receiver", Proc of MIXDES, pp 208-213, Lodz, Poland, 2003.
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27. G Jervan, P Eles, Z Peng, R Ubar, M Jenihhin: "Hybrid BIST time minimization for core-based systems with STUMPS architecture", Proc 18th Int. symposium on defect and fault tolerance in VLSI systems (DFT), Cambridge, Mass, USA, Nov 3-5, 2003.
28. G Jervan, P Eles, Z Peng, R Ubar, M Jenihhin: "Test time minimization for hybrid BIST of core-based systems", Proc. 12th IEEE Asian test symposium (ATS), Xian, China, Nov 17-19, 2003.
29. H Johansson, P Löwenberg: "Linear programming design of linear-phase FIR filters with variable bandwidth", Proc IEEE Symp. Circuits Syst., Bangkok, Thailand, May 25-28, 2003.
30. D Karlsson, P Eles, Z Peng: "Automatic generation of a formal verification bench for a reuse methodology", SSoCC '03, Eskilstuna, April 8-9, 2003.
31. M Karlsson, M Vesterbacka: "A non-overlapping two-phase clock generator with adjustable duty cycle", To appear in Proc GigaNertz 2003 Symp., Linköping, Sweden, Nov 4-5, 2003.
32. M Karlsson, M Vesterbacka: "A robust non-overlapping two-phase clock generator", Proc SSoCC '03, Eskilstuna, Sweden, April 8-9, 2003.
33. M Karlsson, M Vesterbacka, W Kulesza: "Design of digit-serial pipelines with merged logic and latches", To appear in Proc. Norchip 2003, Riga, Latvia, Nov 10-11, 2003.
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40. E Larsson, J Pouget, Z Peng: "Defect probability-based system-on-chip test scheduling", Proc. 6th IEEE international workshop on design and diagnostics of electronics circuits and systems (DDECS '03), Poznan, Poland, April 14-16, 2003.
41. W Li, L Wanhammar: "Low power design for data dependence", Proc SSoCC '03, Eskilstuna, Sweden, April 8-9, 2003.
42. S Natarajan, A Alvandpour: "High performance and SER insensitive memories" to be presented at IMC, Perth, Australia, Dec 2003.
43. S Natarajan, A Alvandpour: "Ultra low power ferroelectric memories for SoC's", to be presented at IMS, Perth, Australia, Dec, 2003.
44. S Natarajan, A Alvandpour: "SoC versus SIP: What makes sense?", to be presented at IMC, Perth, Australia, Dec, 2003.

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62. E Tell, D Liu: "A suitable channel equalization scheme for IEEE 802.11b", Proc. of Swedish system-on-chip conference (SScCC), Eskilstuna, Sweden, April 8-9, 2003.
63. E Tell, M Olausson, D Liu: "A general DSP processor at the cost of 23k gates and 1/2 a man-year design time", Proc. of Int. conference on acoustics, speech and signal processing (ICASSP), Hong Kong, Vol 2, pp 657-660, April 2003.

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65. D Wiklund: "Mesochronous clocking and communication in on-chip networks", Proc. Swedish system-on-chip conference (SSoCC '03), Eskilstuna, April 8-9, 2003.
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Book chapter

1. E Larsson, Z Peng: "An integrated framework for the design and optimization of SOC test solutions", a book chapter in SPC (System-on-Chip) testing for plug and play test automation (K. Chakrabarty, editor), Kluwer Academic Publisher, 2003.
2. U Nordqvist, D Liu: "Chapter 8" to appear in Network Processors: Issue and Practices, Vol 2, November 2003.
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Licenciate - thesis

1. Kalle Folkesson: "ADC modeling for system simulation". LiU-TEK-LIC-2003:26, Thesis No. 1027, June 19, 2003.
2. Weidong Li: "Studies on implementation of low power FFT processors". Linköping studies in science and technology, Thesis No. 1030, 2003.
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PhD - thesis

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