

## ***STRINGENT 2004, Appendix 1, Publications***

### ***Books***

1. Per Löwenborg, Editor & Co-author: "Mixed-Signal Processing Systems", 2004.
2. Paul Pop, Petru Eles and Zebo Peng: "Analysis and Synthesis of Distributed Real-Time Embedded Systems", Kluwer Academic Publishers, 2004.
3. Paul Pop, Petru Eles and Zebo Peng: in "Embedded Systems Design The ARTIST Roadmap for Research and Development" Springer Verlag. (Book chapter).
4. Dake Liu, Eric Tell: "Chapter 23: Low power baseband processor for communications". In the book "Low Power Electronics Design" edited by prof. Christian Piguet, ISBN 0-8493-1941-2.
5. Christer Svensson: "Low-Power and Low-Voltage Communication for SOC's", in C. Piguet, ed. Low-Power Electronics Design, CRC-Press, 2004, ISBN 0-8493-1941-2, (Book chapter).

### ***Journal papers***

1. S. Andersson, and C. Svensson, "An Active Recursive RF Filter in 0.35 $\mu$  m BiCMOS" has been accepted for publication in the journal Analog Integrated Circuits and Signal Processing, Kluwer.
2. A. Andrei, M. Schmitz, P. Eles, Z. Peng, and B. Al-Hashimi, "Overhead-Conscious Voltage Selection for Dynamic and Leakage Energy Reduction of Time-Constrained Systems", IEEE Proceedings Computers & Digital Techniques, special issue with the best contributions from the DATE 2004 (accepted).
3. O. Gustafsson, "Graph-based code word selection for memoryless low power bus coding," Electronics Letters, vol. 40, no. 24, pp. 1531-1532, 25 Nov. 2004.
4. D. Jakonis, K. Folkesson, J. Dabrowski, P. Eriksson, C. Svensson, "A 2.4-GHz RF sampling receiver front-end in 0.18  $\mu$ m CMOS", accepted to IEEE Journal of Solid-State.
5. H. Johansson and P. Löwenborg, "On linear-phase FIR filters with variable bandwidth," IEEE Trans. Circuits Syst. II, vol. 51, no. 4, pp. 181-184, Apr. 2004.
6. H. Johansson, and P. Löwenborg, "Reconstruction of nonuniformly sampled bandlimited signals by means of time-varying discrete-time FIR filters," accepted for publication in J. Applied Signal Processing Special Issue on Frames and Overcomplete Representations in Signal Processing, Communications, and Information Theory.
7. E. Larsson, K. Arvidsson, H. Fujiwara and Z. Peng, "Efficient Test Solutions for Core-Based Designs," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol. 23, No. 5, 2004, pp. 758-775.
8. E. Larsson and H. Fujiwara, "Preemptive System-on-Chip Test Scheduling," IEICE Transactions on Information Systems. Special Issue on Test and Verification of VLSI, Vol. E87-D, No. 3, March 2004, pp. 620-629.
9. P. Löwenborg, H. Johansson, and L. Wanhammar, "First-order sensitivity of complementary diplexers," IEEE Trans. Circuits Syst. II, vol. 51, no. 8, pp. 421-425, 2004.
10. S. Manolache, P. Eles and Z. Peng, "[Schedulability Analysis of Applications with Stochastic Task Execution Times](#)", ACM Transactions on Embedded Computing Systems, volume 3, issue 4, November 2004, pp. 706-735.
11. P. Pop, P. Eles, and Zebo Peng, "Schedulability-Driven Frame Packing for Multi-Cluster Distributed Embedded Systems, ACM Transactions on Embedded Computing Systems (in print).

### **Conference papers**

1. K.O. Andersson and M. Vesterbacka, "A Testbed for Different Codes in Digital-to-Analog Converters," Proc. Swedish System-on-Chip Conf. 2004, Båstad, Sweden, Apr. 13-14, 2004.
2. K.O. Andersson and M. Vesterbacka, "Partial Decomposition of Digital-to-Analog Converters," Proc. IEEE Mediterranean Electrotechnical Conf., vol. 1, pp. 193-196, Dubrovnik, Croatia, May 12-15, 2004.
3. K.O. Andersson and M. Vesterbacka, "A Parameterized Cell-Based Design Approach for Digital-to-Analog Converters," Proc. IEEE 4th Int. Workshop on System-on-Chip for Real-Time Applications, IWSOC'04, pp. 225-228, Banff, Alberta, Canada, July 19-21, 2004.
4. M. Andersson, J. Elbornsson, J-E Eklund, J. Alvebrant, H. Fredriksson, "Verification of a blind mismatch error equalization method for randomly interleaved ADCs using a 2.5 V/12b/30MSs PSAADC", in Proc. of SSOC 2004, p. 4, Båstad, 13-14 April, 2004.
5. S. Andersson, and C. Svensson, "Channel length as a design parameter for low noise wideband LNAs in deep submicron CMOS technologies", in Proc. of 22<sup>nd</sup> Norchip Conference, pp. 123-126, Oslo, Norway, 8-9 November 2004.
6. S. Andersson, and C. Svensson, "Channel length as a design parameter for low noise wideband LNA's in deep submicron CMOS technologies", Swedish System-on-Chip Conference, SSoCC 2004, 4 p., Båstad, Sweden, April 13-14 2004.
7. A. Andrei, M Schmitz, P. Eles, Z. Peng, and B. Al-Hashimi, "Quasi-Static Voltage Scaling for Energy Minimization with Time Constraints", Design Automation and Test in Europe Conference (DATE 2005) (to be published).
8. A. Andrei, M Schmitz, P. Eles, Z. Peng, and B. Al-Hashimi, "Simultaneous Communication and Processor Voltage Scaling for Dynamic and Leakage Energy Reduction in Time-Constrained Systems", Int. Conference on Computer Aided Design (ICCAD 2004), San Jose, USA, Nov. 7-11, 2004, pp. 262-269.
9. A. Andrei, M Schmitz, P. Eles, Z. Peng, and B. Al-Hashimi, "Overhead-Conscious Voltage Selection for Dynamic and Leakage Energy Reduction of Time-Constrained Systems", Design, Automation and Test in Europe (DATE 2004), Paris, France, February 16-20, 2004, pp. 518-523.
10. E. Backenius and M. Vesterbacka, "A Digital Circuit with Relaxed Clocking," Proc. Swedish System-on-Chip Conf. 2004, Båstad, Sweden, Apr. 13-14, 2004.
11. E. Backenius and M. Vesterbacka, "Design of Circuits for a Robust Clocking Scheme," Proc. IEEE Mediterranean Electrotechnical Conf., MELECON'04, vol. 1, pp. 185-188, Dubrovnik, Croatia, May 12-15, 2004.
12. E. Backenius and M. Vesterbacka, "Evaluation of a Clocking Strategy with Relaxed Constraints on Clock Edges," Proc. IEEE Analog and Digital Techniques in Electrical Engineering, TENCON'04, Chiang Mai, Thailand, Nov. 21-24, 2004.
13. H. Bengtson and C. Svensson, "Amplifier stability related to power supply impedance," in Proc. of The 11th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES), pp. 151-156, Szczecin, Poland, 24-26 June 2004.
14. H. Bengtson and C. Svensson, "2.5 Gb/s, 72  $\Omega$ , transimpedance amplifier in 0.35  $\mu\text{m}$  CMOS," in Proc. of the 2004 IEEE 7th International Analog VLSI Workshop (AVLSIWS), pp. 261-266, Macau, 13-15 Oct. 2004.
15. H. Bengtson and C. Svensson, "A scalable and robust rail-to-rail delay cell for DLLs," in Proc. of the IEEE International SOC Conference, pp. 135-136, Santa Clara, USA, 12-15 Sept. 2004.
16. P. Caputa, A. Alvandpour and C. Svensson, "High-speed on-chip interconnect modeling for circuit simulation", in Proc. of 22<sup>nd</sup> Norchip Conference, pp. 143-146, Oslo, Norway, 8-9 November 2004.

17. P. Caputa, M. A. Anders, C. Svensson, R. K. Krishnamurthy, and S. Borkar, "A Low-swing Single-ended L1 Cache Bus Technique for Sub-90nm Technologies", in Proc. of ESSCIRC, pp. 475-477, Leuven, Belgium, 21-23 Sept. 2004.
18. P. Caputa, H. Fredriksson, M. Hansson, S. Andersson, A. Alvandpour, and C. Svensson, "An Extended Transition Energy Cost Model for Buses in Deep Submicron Technologies", in Proc. of The Fourteenth International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2004, pp. 849-858, Santorini, Greece, September 15-17 2004.
19. P. Caputa, A. Alvandpour, and C. Svensson, in Proc. of "High-speed on-chip interconnect modeling for circuit simulation", Swedish System-on-Chip Conference, Båstad, 4 p., 13-14 April 2004.
20. I. Carlson, S. Andersson, S. Natarajan, and A. Alvandpour, "A high density, low leakage, 5T SRAM for embedded caches", in proceedings of European Solid-State Circuits Conference, ESSCIRC, pp. 215-222, Leuven, Belgium, September 21-23 2004.
21. L. A. Cortes, P. Eles and Z. Peng, "Combining Static and Dynamic Scheduling for Real-Time Systems"; Workshop on Software Analysis and Development for Pervasive Systems (SONDA 2004), Invited Paper, Verona, Italy, August 24, 2004, pp. 32-40.
22. L. A. Cortes, P. Eles and Z. Peng, "Quasi-Static Scheduling for Real-Time Systems with Hard and Soft Tasks Design; Automation and Test in Europe (DATE 2004)", Paris, France, February 16-20, 2004, pp. 1176-1181.
23. L. A. Cortes, P. Eles and Z. Peng, "Static Scheduling of Monoprocessor Real-Time Systems composed of Hard and Soft Tasks; The IEEE International Workshop on Electronic Design, Test and Applications (DELTA 2004)", Perth, Australia, January 28-30, 2004, pp. 115-120
24. J. Dabrowski and L. Li, "Signal Path Sensitization for Built-in-Self-Test in Integrated RF Transceivers", in Proc of DDECS'04, pp. 59-66, Stara Lesna, Slovakia, 19-21 April 2004.
25. J. Dabrowski, "Fault Modeling of RF Blocks Based on Noise Analysis", in Proc. of ISCAS'04, pp. I-513-516, Vancouver, Canada, 24-26 May 2004.
26. J. Dabrowski and J. Gonzalez Bayon, "Mixed Loopback BiST for RF Digital Transceivers", in Proc. of DFT'04, pp. 200-288, Cannes, France, 11-13 Oct. 2004.
27. G. Dempster, M. D. Macleod, and O. Gustafsson, "Comparison of graphical and sub-expression elimination methods for design of efficient multipliers," in Proc. Asilomar Conf. Signals, Syst., Comp., Monterey, CA, Nov. 7-10, 2004.
28. S. Edbom and E. Larsson, "An Integrated Technique for Test Vector Selection and Test Scheduling under Test Time Constraint," Proc. IEEE Asian Test Symposium (ATS'04), Kenting, Taiwan, Nov. 15-17, 2004.
29. A. Edman, and C. Svensson, "Timing closure through a globally synchronous, timing partitioned design methodology", in Proc. of 41st Design Automation Conference, pp. 71-74, San Diego, USA, 7-11 June 2004.
30. A. Ehliar and D. Liu, "Benchmarking network processors", Proc of the Swedish System-on-Chip Conference (SSoCC), Båstad, Sweden, 13-15 April, 2004.
31. J. Eilert, A. Ehliar, and D. Liu, "Using low precision floating point numbers to reduce memory cost for MP3 decoding", Proc of the IEEE Int'l Workshop on Multimedia Signal Processing (MMSP), Siena, Italy, Sept. 2004.
32. K. Folkesson, D. Jakonis, J. Dabrowski, and C. Svensson, "Design of RF sampling receiver front-end", in Proceedings of MIXDES 2004, pp. 538-543, Szczecin, Poland, 2004. Outstanding paper Award.
33. K. Folkesson, and C. Svensson, "Robust Multi-Phase Clock Generation with Reduced Jitter", in Proc. of SOCC, pp. 167-168, Santa Clara, USA, 12-15 Sept 2004.
34. K. Folkesson, D. Jakonis, J. Dabrowski, and C. Svensson, "RF-sampling receiver front-end design", in Proceedings of SSoCC'04, 4 p., Båstad, Sweden, 13-14 April 2004.

35. K. Folkesson, C. Svensson, B. Knuthammar, and A. Dreyfert, "A High-Level Dynamic-Error Model of a Pipelined Analog-to-Digital Converter", accepted to ISCAS 2005.
36. H. Fredriksson, and C. Svensson, "Gb/s equalizer for multi-drop memory buses", in Proc of SSoCC 2004, 4 p., Båstad, Sweden, April 13-14 2004.
37. H. Fredriksson, and C. Svensson, "Mixed-signal decision feedback equalizer for multi-drop, Gb/s, memory buses, a feasibility study", in proceedings of SOCC, pp. 147-148, Santa Clara, 13-15 Sept. 2004.
38. O. Gustafsson, H. Johansson, and L. Wanhammar, "MILP design of frequency-response masking FIR filters with few SPT terms," in Proc. 1st Int. Symp. Control, Commun., Signal Processing, Hammamet, Tunisia, Mar. 2124, 2004.
39. O. Gustafsson and L. Wanhammar, "Design of reduced complexity linear-phase polyphase FIR filters using mixed integer linear programming," in Proc. Swedish System-on-Chip Conf., Båstad, Sweden, April 13-14, 2004.
40. O. Gustafsson, A. G. Dempster, and L. Wanhammar, "Multiplier blocks using carry-save adders," in Proc. IEEE Int. Symp. Circuits Syst., Vancouver, Canada, May 23-26, 2004.
41. O. Gustafsson and A. G. Dempster, "On the use of multiple constant multiplication in polyphase FIR filters and filter banks," in Proc. Nordic Signal Processing Symp., Espoo, Finland, June 911, 2004, pp. 53-56.
42. O. Gustafsson, H. Ohlsson, and L. Wanhammar, "Low-complexity constant coefficient matrix multiplication using a minimum spanning tree approach," in Proc. Nordic Signal Processing Symp., Espoo, Finland, June 911, 2004, pp. 141-144.
43. O. Gustafsson, J. O. Coleman, A. G. Dempster, and M D. Macleod, "Low-complexity hybrid form FIR filters using matrix multiple constant multiplication," in Proc. Asilomar Conf. Signals, Syst., Comp., Monterey, CA, Nov. 7-10, 2004.
44. O. Gustafsson, H. Ohlsson, and L. Wanhammar, "Improved multiple constant multiplication using minimum spanning trees," in Proc. Asilomar Conf. Signals, Syst., Comp., Monterey, CA, Nov. 7-10, 2004.
45. M. Hansson, and A. Alvandpour, "A Low Clock Load Conditional Flip-flop", in Proc. of IEEE International System-on-Chip Conference, SoCC, pp. 169-170, Santa Clara, USA, 12-15 September 2004.
46. M. Hansson, and A. Alvandpour, "A Leakage Compensation Technique for Low-Power Dynamic Latches", in Proc. of Swedish System-on-Chip Conference, SSoCC 2004, 4 p., Båstad, Sweden, April 13-14 2004.
47. Z. He, G. Jervan, Z. Peng and P. Eles, "Hybrid BIST Test Scheduling Based on Defect Probabilities," Proc. IEEE Asian Test Symposium (ATS'04), Kenting, Taiwan, Nov. 15-17, 2004, pp. 230-235.
48. R. Häggglund, E. Hjalmarson, and L. Wanhammar, "Yield Enhancement Techniques in Analog Design Automation," Proc. IEEE NorChip Conf., Oslo, Norway, Nov. 8-9, 2004.
49. R. Häggglund, E. Hjalmarson, and L. Wanhammar, "Automated device sizing of analog circuits with yield enhancement", Swedish System-on-Chip Conference, Båstad, Apr. 13-14, 2004.
50. V. Izosimov, P. Pop, P. Eles, and Z. Peng, "Design Optimization of Time- and Cost-Constrained Fault-Tolerant Distributed Embedded Systems", Design Automation and Test in Europe Conference (DATE 2005), accepted.
51. D. Jakonis, K. Folkesson, C. Svensson, J. Dabrowski, and P. Eriksson, "An RF sampling downconversion filter for a receiver front-end", in Proceedings of MWSCAS, pp. I-165-I-168, Hiroshima, Japan, 2004.
52. H. Johansson and P. Löwenborg, "Flexible frequency-band reallocation network based on variable oversampled complex-modulated filter banks", in Proc. IEEE Int. Conf. Acoust. Speech, Signal Processing, Philadelphia, USA, Mar. 2005.
53. H. Johansson, "On the design of IIR bandpass filters with an adjustable bandwidth and centre frequency," in Proc. IEEE Int. Symp. Circuits Syst., Vancouver, Canada, May 2004.

54. H. Johansson and O. Gustafsson, "Mth-band linear-phase FIR filter interpolators and decimators utilizing the Farrow structure," in Proc. IEEE Int. Symp. Circuits Syst., Vancouver, Canada, May 23-26, 2004.
55. H. Johansson and P. Löwenborg, "Reconstruction of nonuniformly sampled bandlimited signals using time-varying discrete-time FIR filters," in Proc. XII European Signal Processing Conf., Vienna, Austria, Sept. 6-10, 2004.
56. H. Johansson and P. Löwenborg, "Reconstruction of periodically nonuniformly sampled bandlimited signals using time-varying FIR filters," in Proc. Fourth Int. Workshop Spectral Methods Multirate Signal Processing, Vienna, Austria, Sept. 11-12, 2004.
57. K. Johansson, O. Gustafsson, and L. Wanhammar, "Power estimation of bit-serial constant-coefficient multipliers," in Proc. Swedish System-on-Chip Conf., Båstad, Sweden, April 13-14, 2004.
58. K. Johansson, O. Gustafsson, and L. Wanhammar, "Switching activity in bit-serial constant coefficient multipliers," in Proc. IEEE Int. Symp. Circuits Syst., Vancouver, Canada, May 23-26, 2004.
59. K. Johansson, O. Gustafsson, A. G. Dempster, and L. Wanhammar, "Algorithm to reduce the number of shifts and additions in multiplier blocks using serial arithmetic," in Proc. IEEE Mediterranean Electrotechnical Conf., Dubrovnik, Croatia, May 12-15, 2004.
60. K. Johansson, O. Gustafsson, and L. Wanhammar, "Low-complexity bit-serial constant-coefficient multipliers," in Proc. IEEE Int. Symp. Circuits Syst., Vancouver, Canada, May 23-26, 2004.
61. K. Johansson, O. Gustafsson, and L. Wanhammar, "Power estimation for ripple-carry adders with correlated input data", Int. Workshop Power Timing Modeling, Optimization, Simulation, Santorini, Greece, Sept. 15-17, 2004.
62. D. Karlsson, P. Eles and Z. Peng, "A Formal Verification Approach for IP-based Designs; Forum on Specification and Design Languages", Lille, Sept. 13-17, France, 2004, pp. 556-557.
63. D. Karlsson, P. Eles and Z. Peng, "A Formal Verification Methodology for IP-based Designs Euromicro Symposium on Digital System Design, Architectures, Methods and Tools", Aug.31 - Sept. 3, Rennes, France, 2004, pp.372-379.
64. D. Karlsson, P. Eles and Z. Peng, "A Formal Verification Methodology for IP-based Designs"; Swedish System-on-Chip Conference 2004, Båstad, Sweden, April 13-14, 2004.
65. M. Karlsson, M. Vesterbacka, and W. Kulesza, "A Method for Increasing the Throughput of Fixed Coefficient Digit-Serial/Parallel Multipliers," Proc. 2004 IEEE Int. Symp. on Circuits and Systems, ISCAS' 04, Vancouver, Canada, May 23-26, 2004.
66. M. Karlsson, M. Vesterbacka, and W. Kulesza, "Pipelining of Digit-Serial Processing Elements in Recursive Digital Filters," Proc. 2004 IEEE Nordic Signal Processing Symp., NORSIG'04, pp. 129-132, Espoo, Finland, June 9-11, 2004.
67. K. Landernäs, J. Holmberg, and O. Gustafsson, "Implementation of bit-level pipelined digit-serial multipliers," in Proc. Nordic Signal Processing Symp., Espoo, Finland, June 9-11, 2004, pp. 125-128.
68. K. Landernäs, J. Holmberg, and M. Vesterbacka, "A High-Speed Low-Latency Digit-Serial Hybrid Adder," Proc. 2004 IEEE Int. Symp. on Circuits and Systems, ISCAS'04, vol. 3, pp. 217-220, Vancouver, Canada, May 23-26, 2004.
69. E. Larsson, "Integrating Core Selection in the SOC Test Solution Design-Flow," Proc. International Test conference (ITC'04), Charlotte, NC, USA, October 2004.
70. A. Larsson, E. Larsson, P. Eles and Z. Peng, "A Technique for Optimization of System-on-Chip Test Data Transportation," Proc. 9<sup>th</sup> IEEE European Test Symposium, Corsica, France, May 23-26, 2004.

71. E. Larsson, J. Pouget and Z. Peng, "Defect-Aware SOC Test Scheduling," Proc. 2004 IEEE VLSI Test Symposium (VTS'04), Napa Valley, USA, April 2004, pp. 359-364.
72. A. Larsson, E. Larsson, P. Eles and Z. Peng, "A Technique for Optimisation of SOC Test Data Transportation," Proc. Swedish System-on-Chip Conference (SSoCC'04), Båstad, Sweden, Apr. 13-14, 2004.
73. E. Larsson, "Core Selection Integrated in the SOC Test Solution Design-Flow," Proc. International Workshop on Test Resource Partitioning (TRP), Napa Valley, USA, April 2004.
74. W. Li and L. Wanhammar, "An offset prefix adder for conversion and addition," in Proc. Swedish System-on-Chip Conf., Båstad, Sweden, April 13-14, 2004.
75. L. Lindgren, "Elimination of Quantization Effects in Measured Temporal Noise", in Proceedings of 2004 IEEE International Symposium on Circuits and System (ISCAS04), Vancouver, volume IV, pp. IV-932-935, May 23-26 2004, Received the Sensory Systems Track Best Paper Award.
76. T. Lindkvist, J. Löfvenberg, and O. Gustafsson, "Deep sub-micron bus invert coding," in Proc. Nordic Signal Processing Symp., Espoo, Finland, June 9-11, 2004, pp. 133-136.
77. T. Lindkvist, J. Löfvenberg, H. Ohlsson, K. Johansson and L. Wanhammar, "A power-efficient, low-complexity, memoryless coding scheme for buses with dominating inter-wire capacitance," IEEE Int. Workshop on System-on-Chip for Real-Time Appl., Banff, Canada, July 19-21, 2004, pp. 257-262.
78. 2004, HangZhou, China, 3-5 November, 2004.
79. P. Löwenborg and H. Johansson, "Minimax design of linear-phase FIR filters with adjustable bandwidths," in Proc. IEEE Int. Symp. Circuits Syst., Vancouver, Canada, May 2004.
80. R. Malmqvist, M. Hansson, C. Samuelsson, et. al, "Some Important Aspects on the Design of Active Microwave Filters using Standard RF Silicon Process Technologies", European Microwave Conference, EuMC 2004, pp. 941-944, Amsterdam, The Netherlands, 12-14 Oct. 2004.
81. S. Manolache, P. Eles, and Z. Peng: "Optimization of Soft Real-Time Systems with Deadline Miss Ratio Constraints", 10<sup>th</sup> IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS04), pp. 562-570, May 2004, Toronto, On., Canada
82. B. Mesgarzadeh, C. Svensson, and A. Alvandpour, "A New Mesochronous Clocking Scheme for Synchronization in SoC", in Proc. of IEEE Symp. on Circuits and Systems (ISCAS'04), pp. II -605- D. Liu, E. Tell, and A. Nilsson: (Special invited) Implementation of programmable Baseband processors, CCIC 608, Vancouver, Canada, 23-26 May 2004.
83. B. Mesgarzadeh, "A CMOS Implementation of Min-Max Circuits in Current mode and A Sample Fuzzy Application", IEEE International Conf. on Fuzzy Systems, p. 170, Budapest, Hungary, 25-29 July 2004.
84. R. Mohamed, Z. Peng and P. Eles, "A Heuristic for Wiring-Aware Built-In Self-Test Synthesis," Proc. EUROMICRO Symposium on Digital System Design, Rennes, France, Aug. 31- Sept. 3, 2004.
85. R. Mohamed, Z. Peng and P. Eles, "A Heuristic for Wiring-Aware Built-In Self-Test Synthesis," Proc. Swedish System-on-Chip Conference (SSoCC'04), Båstad, Sweden, Apr. 13-14, 2004.
86. R. Mohamed, Z. Peng and P. Eles, "A Wiring-Aware Approach to Minimizing Built-In Self-Test Overhead," Proc. IEEE International Workshop on Electronic Design, Test and Applications (DELTA 2004), Perth, Australia, January 28-30, 2004, pp. 413-415.
87. S. Natarajan, and A. Alvandpour, (invited paper), "Mainstream Memory Technologies in Deep Submicron", in Proceeding of the 12th IEEE Mediterranean Electrotechnical Conference, MELECON, pp. 175-178, Dubrovnik, Croatia, 12-15 May 2004.
88. A. Nilsson and D. Liu, "Processor friendly peak-to-average reduction in multi-carrier systems", SSoCC'04, Båstad, Sweden, April 13-14, 2004.

89. A. Nilsson, E. Tell, and D. Liu, "An accelerator structure for programmable multi-standard baseband processors", WNET2004, Banff, AB, Canada, July 2004.
90. H. Ohlsson, O. Gustafsson, and L. Wanhammar, "Implementation of low-complexity FIR filters using difference methods," in Proc. Swedish System-on-Chip Conf., Båstad, Sweden, April 13-14, 2004.
91. H. Ohlsson, O. Gustafsson, and L. Wanhammar, "A shifted permuted difference coefficient method," in Proc. IEEE Int. Symp. Circuits Syst., Vancouver, Canada, May 23-26, 2004.
92. H. Ohlsson, O. Gustafsson, and L. Wanhammar, "Implementation of low-complexity FIR filters using a minimum spanning tree," in Proc. IEEE Mediterranean Electrotechnical Conf., Dubrovnik, Croatia, May 12-15, 2004, pp. 261-264.
93. H. Ohlsson, B. Mesgarzadeh, K. Johansson, O. Gustavsson, P. Löwenborg, H. Johansson, and A. Alvandpour, "A 16 GSPS 0.18  $\mu\text{m}$  CMOS decimator for single-bit  $\Sigma\Delta$ -modulation.
94. M. Olsson, P. Löwenborg, and H. Johansson, "Scaling and round-off noise in multistage interpolators and decimators," in Proc. Fourth Int. Workshop Spectral Methods Multirate Signal Processing, Vienna, Austria, Sept. 11-12, 2004.
95. M. Olsson and H. Johansson, "Blind OFDM carrier frequency offset estimation by locating null subcarriers," in Proc. 9th Int. OFDM-Workshop, Dresden, Germany, Sept. 15-16, 2004.
96. M. Olsson, P. Löwenborg, and H. Johansson, "Scaling of multistage interpolators," in Proc. XII European Signal Processing Conf., Vienna, Austria, Sept. 6-10, 2004.
97. P. Pop, P. Eles, Z. Peng, and V. Izosimov, "Schedulability-Driven Partitioning and Mapping for Multi-Cluster Real-Time Systems", 16<sup>th</sup> Euromicro Conference on Real-Time Systems, Catania, Sicily, Italy, June 30-July 2, pp. 91-100, 2004.
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99. T. Pop, P. Eles, and Z. Peng, "Design Optimization of mixed Time/Event-Triggered Distributed Embedded Systems", Swedish System-on-Chip Conference 2004, Båstad, April 13-14, 2004.
100. Svensson, (invited paper), "Synchronous latency insensitive design", in Proc. of 10<sup>th</sup> IEEE International Symposium on Asynchronous Circuits and Systems, p. 3, Crete, Greece, 19-23 April, 2004.
101. Säll and M. Vesterbacka, "Silicon-on-Insulator CMOS Technology for System-on-Chip," Proc. Swedish System-on-Chip Conf. 2004, Båstad, Sweden, Apr. 13-14, 2004.
102. Säll, M. Vesterbacka and K.O. Andersson, "A Study of Digital Decoders In Flash Analog-To-Digital Converters," Proc. IEEE Int. Symp. on Circuits and Syst., vol. 1, pp. 129-132, Vancouver, Canada, May 2004.
103. Säll, K.O. Andersson, and M. Vesterbacka, "A Dynamic Element Matching Technique for Flash Analog-to-Digital Converters," Proc. 2004 IEEE Nordic Signal Processing Symp., NORSIG'04, pp. 137-140, Espoo, Finland, June 9-11, 2004.
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105. E. Säll and M. Vesterbacka, "A Multiplexer Based Decoder for Flash Analog-to-Digital Converters," IEEE Analog and Digital Techniques in Electrical Engineering, TENCON'04, Chiang Mai, Thailand, Nov. 21-24, 2004.
106. E. Tell and D. Liu, "A Hardware Architecture for a Multi Mode Block Interleaver" Proc of the International Conference on Circuits and Systems for Communications (ICCSC), Moscow, Russia, June 2004.

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