Cycle-Accurate Test Power Modeling and Its Application to SoC Test Architecture Design and Scheduling

Soheil Samii, Mikko Selkälä, Erik Larsson, Krishnendu Chakrabarty, and Zebo Peng

***Abstract*—Concurrent testing of the cores in a core-based system-on-chip reduces the test application time but increases the test power consumption. Power models, test architecture design, and scheduling algorithms have been proposed to schedule the tests as concurrently as possible while respecting the power budget. The commonly used global peak power model, with a single value capturing the power dissipated by a core when tested, is simple for a scheduling algorithm to handle but is pessimistic. In this paper, we propose a cycle-accurate power model with a power value per clock cycle and a corresponding test architecture design and scheduling algorithm. The power model takes into account the switching activity in the scan chains caused by both the test stimuli and the expected test responses during scan-in, launch-and-capture, and scan-out. Furthermore, we allow a unique power model per wrapper-chain configuration as the activity in a core will be different depending on the number of wrapper chains at a core. Through circuit simulations on ISCAS'89 benchmarks, we demonstrate a high correlation between the real test power dissipation and our cycle-accurate test power model. Extensive experiments on ITC'02 benchmarks and an industrial design show that the testing time can be reduced substantially by using the proposed cycle-accurate test power model.**

***Index Terms*—Power constraint, power estimation, scan chain, system-on-chip (SoC), test architecture design, test power, test scheduling.**

I. Introduction

Long test application times for systems-on-chip (SoCs) are a major problem for core-based SoCs. This problem can be addressed by concurrent testing, in which several cores are tested at the same time. Concurrent testing leads to an increased switching activity in the chip (hence higher power consumption). Exceeding the power limit can, in turn, damage the circuit under test [1].

The modeling of test power consumption is difficult. The gates in a circuit do not dissipate the same amount of power during switching, and the gates with the same applied input stimuli switch at different probabilities. Table I lists some power properties capturing these issues, where $P_{0\rightarrow 1}$ is the probability that a transition from 0 to 1 occurs at the output with random input.

TABLE I
AMS c35 Core Cells (The Output Load Is 20 fF for Each Core Cell)

Gate	Power [μW/Mhz]	$P_{0\rightarrow 1}$
CLKIN1	0.32	25%
NAND21	0.35	19%
NOR21	0.43	19%
XNOR21	0.50	50%
XOR21	0.61	50%
DFS1	1.27	–

Chou *et al.* [1] approximated the test power consumption for each core to a single fixed value, the peak power consumption. Fig. 1 shows the actual and the modeled power consumption based on a single value for a design example. The false power is the mismatch between the actual and the modeled power consumption.

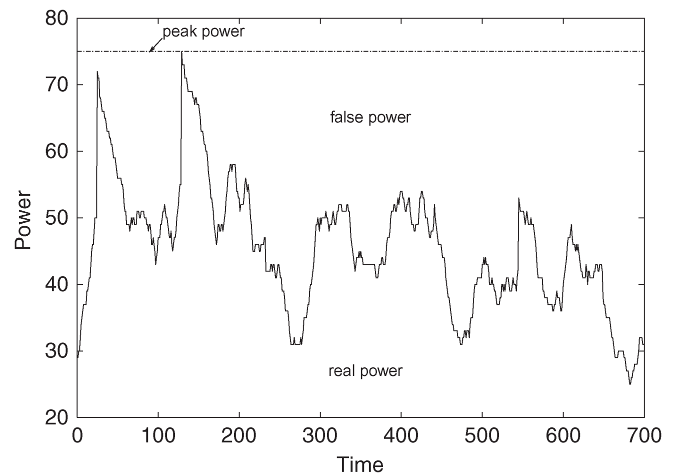

Fig. 1. Global peak power model.

The single-value power model is pessimistic and therefore leads to not as low test time as would be possible, but it guarantees that the power limit will not be violated. Furthermore, the model is very simple to be handled by a test scheduling algorithm. Huang *et al.* [2] and Pouget *et al.* [3] studied power-constrained SoC test scheduling using the global peak model.

In this paper, we propose a cycle-accurate test power model with a designated power value per clock cycle. We consider, at each clock cycle, the scan-chain switching activity produced by both the test stimuli and the test responses during scan-in and scan-out, as well as during launch-and-capture. In addition, as the same test stimuli and test responses for a given core may consume different amounts of power depending on the number of wrapper chains, we have a power profile for each wrapper-chain configuration; hence, there are several power profiles for each core. To evaluate whether the power model is appropriate for power-constrained test scheduling, we perform detailed power simulations using state-of-the art tools for transistor-level simulation of electronic circuits. We also propose a power-constrained test architecture design and test scheduling algorithm. The experimental results on several ITC'02 benchmarks, and an industrial design, show that, by making use of the proposed power modeling technique, the test application time can be reduced substantially, compared with using the single-value power model, without any notable increase in execution time of the algorithm.

The remainder of this paper is organized as follows. Section II describes the proposed test power modeling technique, whereas Section III presents the power-aware test architecture design and scheduling heuristic. Section IV presents the results, whereas Section V concludes this paper.

II. Cycle-Accurate Power Modeling

The power consumption is the sum of a static part and a dynamic part. For most current CMOS technologies, the static part is constant and dominated by the dynamic part. The dynamic part is proportional

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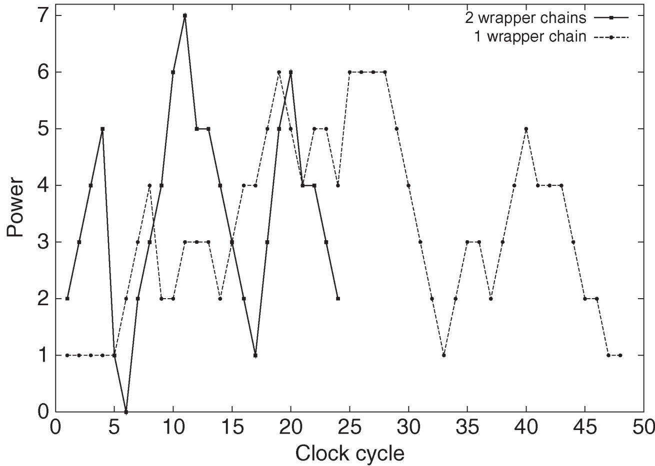

Fig. 2. Power profiles (scan in and scan out) for the two different wrapper-chain configurations when tested with five test patterns.

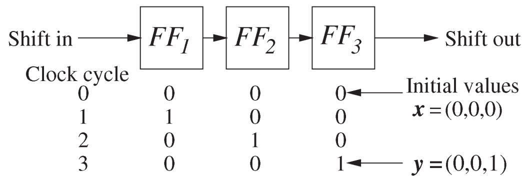

Fig. 3. Example of scan-chain transitions.

to the switching activity α (the number of zero-to-one and one-to-zero transitions) in the circuit [4]; hence, we concentrate on determining α on the basis of the given test stimuli and the given expected test responses for a core. Let us consider a core with two chains to illustrate how the power profiles vary depending on the wrapper-chain configuration. The scan chains may be configured into two wrapper chains or as a single wrapper chain. We consider that the core is tested with five test patterns. Fig. 2 shows the power profile for each wrapper-chain configuration. Note that the two power profiles are different in both the time domain (horizontal axis) and the power domain (vertical axis).

Testing a core, equipped with scan chains, means shifting in a test stimulus to the core's scan chains, launching the test (one capture cycle), after which the test response is shifted out while shifting in the next test stimulus. Transitions occur due to the shifting in of the test stimuli, launch-and-capture, and the shifting out of the test responses.

Consider the scan chain in Fig. 3 with initial values 0 in all flip-flops, i.e., $\boldsymbol{x} = (0, 0, 0)$. We show how the values in the flip-flops change while shifting in the bit sequence $\boldsymbol{y} = (y_1, y_2, y_3) = (0, 0, 1)$, starting with $y_3 = 1$. The sequence $\boldsymbol{y}$ can be viewed as the current test stimulus for the scan chain. Similarly, $\boldsymbol{x}$ is the produced test response from the previous captured test stimulus. For example, at the second clock cycle (from one to two), there are two transitions (at FF_1 and FF_2). In general, shifting in m bits in a scan chain of arbitrary length takes m clock cycles. We model the transitions during shifting according to the following definition.

We now consider testing a core and thus assume that the scanned elements (wrapper input/output cells and scan chains) are connected as w wrapper chains. The scan-in and scan-out times of the core are $\mathrm{si} = \max\{\mathrm{si}_1, \ldots, \mathrm{si}_w\}$ and $\mathrm{so} = \max\{\mathrm{so}_1, \ldots, \mathrm{so}_w\}$, respectively, where si_k and so_k are the scan-in and scan-out of wrapper chain k, respectively. Depending on which test pattern that is applied, the shift-in time is different. For some wrapper chains, we need to shift in some idle bits before shifting in the actual test stimulus. The

1: **repeat**
2: Find TAM_{max} with current most scheduled time
3: Schedule core C_I on TAM_J such that
$$\tau\left(\mathrm{TAM}_{max}\right) - \left(\tau\left(\mathrm{TAM}_J\right) + \tau\left(C_I^{(w_J)}\right)\right)$$
is minimum, > 0, and without exceeding $P_{\max}$.
4: **if** there is no such pair (C_I, TAM_J) **then**
5: **for all** unscheduled cores C_i **do**
6: Choose TAM_{J_i} such that
$$\tau\left(\mathrm{TAM}_{J_i}\right) + \tau\left(C_I^{(w_{J_i})}\right) - \tau\left(\mathrm{TAM}_{max}\right)$$
is minimum, and without exceeding $P_{\max}$.
7: **end for**
8: Choose an unscheduled core C_I which maximizes $Area\left(P_{I,J_I}\right)$; schedule C_I on TAM_{J_I}.
9: **end if**
10: **until** all cores are scheduled

Fig. 4. Test scheduling algorithm for a given fixed-width test bus architecture.

testing time (in clock cycles) [5] for a core with p test patterns is calculated as

$$\tau = (\max(\mathrm{si}, \mathrm{so}) + 1) \cdot p + \min(\mathrm{si}, \mathrm{so}). \quad (1)$$

Thus, we calculate the switches for each wrapper-chain configuration, and we have different power profiles for different wrapper-chain configurations (connections of the wrapper input/output cells and scan chains). Moreover, the number of transitions during a launch-and-capture cycle is given as the number of bits that differs in the test stimulus and its corresponding expected test response. Details can be found in [6]. Note that the correlation between scan shift power and total test power was demonstrated in [7].

III. Test Architecture Design and Scheduling

We propose a test architecture design and test scheduling heuristic. We exhaustively search all possible fixed-width test bus architectures for a given test-access-mechanism (TAM) width. For each such test architecture, we schedule the cores with the goal of minimizing the testing time under the given power constraint. This subproblem is now stated in detail.

Problem formulation. Given is an SoC with N cores $C_1, \ldots, C_N$, a maximum power limit $P_{\max}$, and a test bus architecture with M TAMs, where w_j is the width of TAM_j. For each core, design a wrapper (partition the scan chains and wrapper cells into a given number of wrapper chains), assign the core to a TAM, and determine the order of test execution such that the total testing time of the SoC is minimized while the test power consumption does not exceed $P_{\max}$. ■

The power curve for a core depends on the switches caused by the test stimuli and the test responses. The transitions also depend on the number of wrapper chains as the wrapper-chain configuration determines the organization of test bits. We have, for the subproblem of finding the wrapper-chain configurations for a core, used the Design_Wrapper algorithm by Iyengar *et al.* [8]. Fig. 4 shows the pseudocode for the test scheduling algorithm. In Table II, we have collected explanations of some of the notations that are used in the algorithm description.

The main idea of the heuristic is to select a core and a TAM such that we get *best fit* to the current schedule (initially empty). This is shown in Fig. 5, where TAM 1 is used and there are two alternatives—A and B for TAM 2. For this example, core B will be scheduled because it gives best fit to the current schedule, i.e., $\Delta t_B < \Delta t_A$.

The scheduling algorithm keeps track of the total-power-consumption profile for the current test schedule. The total power

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TABLE II
NOTATIONS FOR THE SCHEDULING ALGORITHM

Notation	Description
$C_i^{(w_j)}$	Core i with wrapper designed by Design_Wrapper [8] and wrapper width w_j.
$P_{i,j}$	The test power consumption function for core $C_i^{(w_j)}$.
$\tau\left(C_i^{(w_j)}\right)$	Testing time for core $C_i^{(w_j)}$ according to equation (1).
$\tau(\mathrm{TAM}_j)$	Scheduled time on TAM_j. This is initially zero.
$Area(P_{i,j})$	The area under the graph of the discrete function $P_{i,j}$, that is, $\sum_k P_{i,j}(k)$.

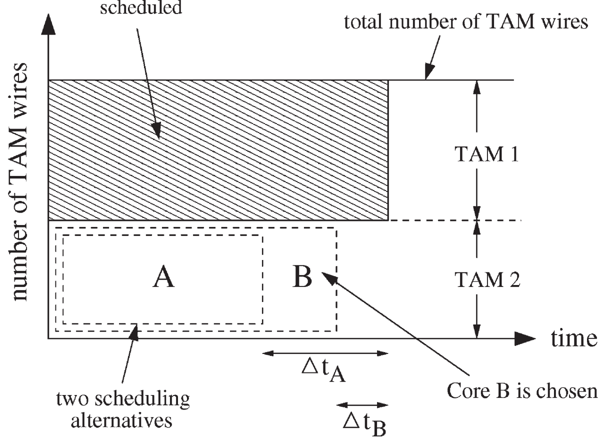

Fig. 5. Illustration of the best fit principle used in the test scheduling algorithm.

consumption is initially zero because no tests are scheduled at the beginning of the algorithm. When a core is considered for scheduling, for example, core $C_i^{(w_j)}$, the corresponding power-consumption function $P_{i,j}$ is accumulated to the total-power-consumption profile, after which the power constraint is checked (lines 3 and 6 in Fig. 4). For the global peak power model, this is fast because we only need to keep track of one value per test, i.e., $P_{i,j}$ is a constant function. For the proposed cycle-accurate model, however, the power-consumption function $P_{i,j}$ is nonconstant and given by the cycle-accurate test power modeling technique described in Section II. Therefore, we need to check each clock cycle, and consequently, this will have a larger impact on the runtime of the test scheduling heuristic. The computational complexity of the test scheduling heuristic, given a test architecture, is

$$\underbrace{O(M)}_{\text{line 2}} + \underbrace{O(N\cdot M)}_{\text{line 3}} + \underbrace{O(N\cdot M) + O(N)}_{\text{lines 4-9}} = O(N\cdot M)$$

where we have shown the line numbers in Fig. 4. Thus, the overall complexity is $O(N \cdot M)$, where N is the number of cores and M is the number of TAMs. The test architecture exploration is done exhaustively for a given number of TAM wires; thus, the complexity is combinatorial in the number of TAM wires.

IV. EXPERIMENTAL RESULTS

We have conducted two sets of experiments. The first experiment targets the correlation between the real test power and the cycle-accurate test power model. The second experiment evaluates the power model for test architecture design and test scheduling with power constraints.

TABLE III
TRANSITION COUNT VERSUS REAL TEST POWER FOR s5378

Scan-in	Scan-out	Total	Power [mW]
3276	3276	6552	38.92
1680	3276	4956	31.95
1680	1680	3360	24.71
720	1680	2400	20.26
720	720	1440	16.63
320	720	1040	13.99
320	320	640	11.34

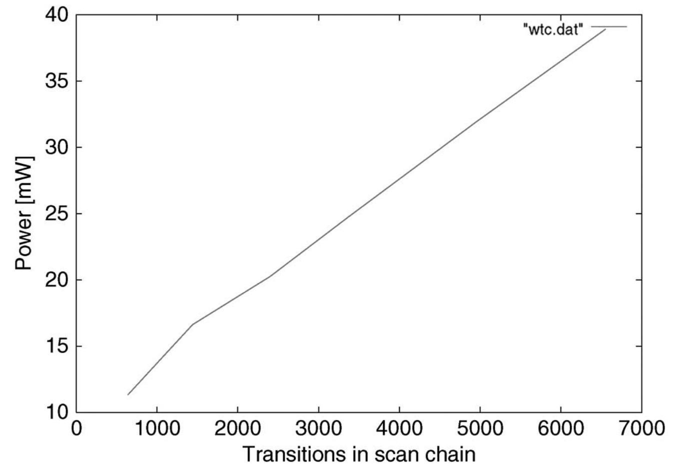

Fig. 6. Total transition count versus power dissipation for s5378.

TABLE IV
PEARSON COEFFICIENTS FOR THE THREE ISCAS'89 CIRCUITS

Circuit	Pearson coefficient
s1423	0.997
s3271	0.999
s5378	0.999

A. Test Power Model Correlation

In our test power simulations, we used the ISCAS circuits s1423, s3271, and s5378. We used the tool LeonardoSpectrum to synthesize the designs into gate-level netlists using the cell library Hit-Kit 3.60-μm CMOS process. DFTAdvisor was used to insert scan cells, and FlexTest was used for automatic test-pattern generation.

We performed two types of simulations. The first simulation used ModelSim, aiming at extracting information about the switching activity in the three circuits. During the simulation, the number of transitions was counted. We also counted the transitions due to scan-in and scan-out separately. For the second experiment, we simulated the real test power consumption for the circuits. We used the tool Affirma Spectre Circuit Simulator. In both simulations, we considered both the test stimuli and the test responses. The results are, due to space limitations, only presented for one circuit (Table III). The first two columns show the transition counts for scan-in and scan-out separately, whereas the third column shows the total transition count. The total transition count is then compared to the real power dissipation in the fourth column. In the table, we can see that a power model that only considers the scan-in transitions does not correlate with the test power dissipation. For example, the first two rows in Table III show that the scan-in transitions are equal, but the test power dissipation values for

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TABLE V
POWER-CONSTRAINED TEST SCHEDULING ON d695 (THE AVERAGE IMPROVEMENT IS 10.4%)

	$P_{\max}$= 1500				$P_{\max}$= 1800			
w_{TAM}	GP	CA	$\Delta t/t_{\mathrm{GP}}$	$\Delta t/t_{\mathrm{LB}}$	GP	CA	$\Delta t/t_{\mathrm{GP}}$	$\Delta t/t_{\mathrm{LB}}$
16	47009	44936	4.4 %	9.7 %	45466	44502	2.1 %	8.7 %
24	31458	30663	2.5 %	–	30926	30663	0.9 %	–
32	27544	23169	15.9 %	13.1 %	25048	22544	10.0 %	10.1 %
40	23937	19200	19.8 %	–	21344	18799	11.9 %	–
48	20842	17013	18.4 %	24.2 %	19607	16686	14.9 %	22.2 %
56	18909	15230	19.5 %	–	18553	13185	28.9 %	–
64	16875	12941	23.3 %	26.3 %	16450	11526	29.9 %	12.5 %
	$P_{\max}$= 2000				$P_{\max}$= 2500			
w_{TAM}	$\Delta t/t_{\mathrm{LB}}$	GP	CA	$\Delta t/t_{\mathrm{GP}}$	$\Delta t/t_{\mathrm{LB}}$	GP	CA	$\Delta t/t_{\mathrm{GP}}$
16	44870	44502	0.8 %	8.7 %	44502	44502	0 %	8.7 %
24	30926	30506	1.4 %	–	30926	30336	1.9 %	–
32	25048	22544	10.0 %	10.1 %	23525	22544	4.2 %	10.1 %
40	20925	18799	10.2 %	–	18988	18799	1.0 %	–
48	18553	16506	11.0 %	20.8 %	16506	16506	0 %	20.8 %
56	17013	13185	22.5 %	–	14834	13185	11.1 %	–
64	14397	11526	19.9 %	12.5 %	13098	11526	12.0 %	12.5 %

the two cases are different. Similarly, only considering the scan-out transitions leads to a power model that does not correlate with the test power simulations. This can, for example, be seen on the second to the fifth line in Table III. The last two columns in the table are shown in Fig. 6. The figure shows an almost linear correlation between our test power model and the real power simulations.

Finally, we have used the Pearson coefficient [9] to quantify the correlation between our test power model and the real power. The obtained values for the three circuits considered in the experiments are listed in Table IV. The coefficients are close to one, indicating a close linear correlation between our test power model and the real test power dissipation.

B. Power-Constrained Test Architecture Design and Test Scheduling

We present here the experimental results that we obtained for comparing the two power models. We used the ITC'02 benchmarks d695, p22810, and p93791, as well as an industrial design (eight cores) (due to space limitations, results for p93791 are excluded but can be found in [6]). For d695 and the industrial design, we used real test data and filled the unspecified bits ("don't care" bits) in the test stimuli according to minimum transition fill and the expected test responses in the most pessimistic way (maximum transition fill). For p22810 and p93791, no netlists are available; therefore, we filled the given number of test patterns of the given length with randomly generated test data.

The experiments were conducted with different values of $P_{\max}$—the maximum allowed power consumption—and w_{TAM}—the total number of available TAM wires. For each w_{TAM}, we ran the test scheduling algorithm exhaustively on all possible fixed-width test bus architectures with a given maximum number of TAMs. The maximum numbers of TAMs for d695, p22810, and p93791 were set to five, four, and three, respectively. The maximum number of TAMs for the industrial design was also set to three.

The CPU times for test scheduling, where the power profiles for each wrapper-chain configuration are provided and the test architecture (TAM partitioning) is given, is low (in seconds only). As we try all possible TAM partitions (for a given maximum number of TAMs), the runtime for test scheduling and TAM architecture design is higher (up to hours). The CPU time to construct the power profile for a given wrapper-chain configuration is reasonable (in minutes); however, as all configurations are needed, it becomes time consuming (up to hours).

We have collected the testing times in Tables V–VII, where GP and CA indicate the global peak power model and the proposed cycle-accurate test power model, respectively. We have also included the relative improvements of the cycle-accurate power model compared with the global peak power model ($\Delta t/t_{\mathrm{GP}} = (t_{\mathrm{GP}} - t_{\mathrm{CA}})/t_{\mathrm{GP}}$, where t_{GP} and t_{CA} are the testing times obtained from our test scheduling algorithm when we use the global peak power model and the proposed cycle-accurate model, respectively). Furthermore, we were also interested in the difference between the lower bounds [10] on the testing times and the testing times obtained by using the cycle-accurate model. Thus, we have included in Tables V and VI the relative difference between our testing times and the lower bounds; the relative difference is $\Delta t/t_{\mathrm{LB}} = (t_{\mathrm{CA}} - t_{\mathrm{LB}})/t_{\mathrm{LB}}$. Note that, for some values of w_{TAM}, there are no lower bounds available. In the tables, we therefore mark those cases with "–." By comparing with the lower bounds, we quantify the quality of our results.

TABLE VI
POWER-CONSTRAINED TEST SCHEDULING ON p22810 (THE AVERAGE IMPROVEMENT IS 11.9%)

	$P_{\max}$= 3000			
w_{TAM}	GP	CA	$\Delta t/t_{\mathrm{GP}}$	$\Delta t/t_{\mathrm{LB}}$
8	1012296	901607	10.9 %	–
16	664511	536978	19.2 %	28.0 %
24	607451	395389	34.9 %	–
32	543358	349530	35.7 %	66.7 %
40	427876	314067	26.6 %	–
48	363299	287642	20.8 %	105.6 %
56	362487	280548	22.6 %	–
64	350162	280548	19.9 %	167.5 %
	$P_{\max}$= 5000			
w_{TAM}	GP	CA	$\Delta t/t_{\mathrm{GP}}$	$\Delta t/t_{\mathrm{LB}}$
8	893226	893231	0 %	–
16	504509	458812	9.1 %	9.4 %
24	365562	331169	9.4 %	–
32	320386	275106	14.1 %	31.2 %
40	289649	240829	16.9 %	–
48	229998	225179	2.1 %	61.0 %
56	219244	215183	1.9 %	–
64	219244	197593	9.9 %	88.4 %
	$P_{\max}$= 8000			
w_{TAM}	GP	CA	$\Delta t/t_{\mathrm{GP}}$	$\Delta t/t_{\mathrm{LB}}$
8	893296	881724	13.0 %	–
16	450546	450051	0.1 %	7.3 %
24	329419	308374	6.4 %	–
32	260711	241841	7.2 %	15.3 %
40	241182	199748	17.2 %	–
48	216632	184728	17.1 %	32.1 %
56	207606	166585	19.8 %	–
64	185309	160485	13.4 %	53.0 %

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TABLE VII
POWER-CONSTRAINED TEST SCHEDULING ON THE INDUSTRIAL DESIGN (THE AVERAGE IMPROVEMENT IS 43.1%)

	P_{max}= 12000		
w_{TAM}	GP	CA	$\Delta t/t_{GP}$
24	153410308	62299271	59.4 %
32	76859936	47860926	37.7 %
40	76859936	47860926	37.7 %
48	76859936	47860926	37.7 %

We can see that using the cycle-accurate power model results in testing times that are closer to the lower bounds compared with using the global peak power model.

V. CONCLUSION

We proposed a test power model with a power value per clock cycle that takes into account the scan-chain switching activity generated by test stimuli and test responses. Furthermore, the model provides a separate power profile per wrapper-chain configuration. Through detailed power simulations, we demonstrated a high correlation between the real test power dissipation and our cycle-accurate power model. We proposed a SoC test architecture design and test scheduling algorithm which makes use of our test power model. We made extensive experiments on several ITC'02 benchmarks and an industrial design, where we compared the testing time when using a single-value (global peak) power model and the proposed cycle-accurate power model. The presented results demonstrate that significant testing time can be saved by making use of our more elaborate power model.

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A Synthesis Tool for CMOS RF Low-Noise Amplifiers

Gülin Tulunay and Sina Balkır

***Abstract*—A stand-alone design automation tool tailored for radio frequency (RF) complementary metal–oxide–semiconductor (CMOS) low-noise amplifier (LNA) designs is presented. Rather than relying on commercially available circuit simulators such as *Spectre* or *Hspice*, the presented synthesis tool is self-contained with its own built-in modules for faster optimization. Foundry-provided silicon-verified RF device models are incorporated into the synthesis procedure for accurate parasitic modeling. The proposed synthesis tool can be used as an independent circuit design environment for LNAs or, alternatively, as an auxiliary tool generating an initial design for a commercial design environment to reduce design time. To validate the proposed approach, an LNA operating at 900 MHz is synthesized and fabricated in a 0.25-μm CMOS technology. Measurement results are presented, which shows the viability of the proposed synthesis tool.**

***Index Terms*—Low-noise amplifier (LNA), noise figure (NF), radio frequency (RF) circuit synthesis, simulated annealing (SA), Volterra series.**

I. INTRODUCTION

With the desire for high integration and low power consumption, the demands on the performance specifications of each radio frequency (RF) functional building block are constantly increasing. Although RF blocks make up a small portion of the whole system, their design time and cost are relatively high compared to their analog and digital counterparts. In addition, as the operating frequency gets higher, the effects of parasitics make the design of RF blocks even more challenging.

The design of low-noise amplifiers (LNAs) involves the achievement of several design goals. Typical design strategies try to minimize noise figure (NF) [1], [2], whereas others try to improve linearity [3] or reduce power [4]. However, optimal solutions involving several design constraints are hard to achieve, and much of the effort is based on experience because systematic design methodologies for RF integrated circuit (RFIC) designs are not readily available. Synthesis tools for the design of RF blocks need to be developed to deal with the increasing complexity of RFICs and to simultaneously consider multiple specifications for rapid design times.

The optimization of RFICs has been addressed in the past by several researchers. Most of the work focused on the optimization of power amplifiers [5]–[8] that employ simulation-based methods. In [9] and [10], equation-based optimization tools for *LC* oscillators are presented. In [11], a simulation-based LNA synthesis tool is proposed. The synthesis tool in [12] relies on a hierarchical analog performance estimator, which is based on a knowledge-based approach and heuristics. Symbolic performance models are used in [13] to estimate the behavior of an LNA. Numerical analysis is required at each iteration to compute the transistor small-signal parameters and nonlinearity coefficients. Bhaduri *et al.* [14] proposes a simulation-based approach with simulated annealing (SA) as the search algorithm. In [15], a simulation-based RFIC synthesizer based on an improved genetic algorithm (GA) is presented. In [16], knowledge-based behavioral models are used for circuit evaluation with a GA as the optimization

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