An Improved Estimation Technique for Hybrid BIST Test Set Generation

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Abstract[1]. *This paper presents an improved estimation technique for hybrid BIST test set generation. In a hybrid BIST approach the test set is assembled from pseudorandom and deterministic test patterns. The efficiency of the hybrid BIST approach is determined by the ratio of those test patterns in the final test set. Unfortunately, exact algorithms for finding the optimal test sets are computationally very expensive. And several heuristics have been developed to address this problem based on estimation methods. In this paper we propose an improved estimation technique for fast generation of the hybrid test set. The technique is based on fault simulation results, and experiments have shown that the proposed technique is more accurate than the estimation methods proposed earlier.*

1. Introduction

Testing of systems-on-chip (SoC) is a problematic and time-consuming task, mainly due to their complexity and high integration density [1]. To test individual cores of a SoC the test pattern source and sink have to be available together with an appropriate test access mechanism (TAM) [2]. Due to the rapid increase of chip speed and test data volume, the traditional Automatic Test Equipment (ATE) based solution is becoming increasingly expensive and inaccurate. Therefore, in order to apply at-speed tests and to keep the test costs under control, built-in self-test (BIST) solutions are becoming a mainstream technology for testing such complex systems.

BIST for digital logic (logic BIST) uses mostly pseudorandom tests. Due to several reasons, like very long test sequences, and random pattern resistant faults, this approach may not always be efficient. One solution to the problem is to complement pseudorandom test patterns with deterministic test patterns, applied from an on-chip memory or, in special situations, from an ATE. This approach is usually referred to as hybrid BIST [3].

One of the important parameters influencing the efficiency of a hybrid BIST approach is the ratio of pseudorandom and deterministic test patterns in the final test set. As the amount of resources on the chip is limited, the final test set has to be designed in such a way that the deterministic patterns fit into the on-chip memory. At the same time, the testing time must be minimized in order to reduce the testing cost and time-to-market.

Finding the best ratio of these test sets is computationally very expensive and therefore several methods for fast estimation of the ratio of the pseudorandom and deterministic test patterns in the final hybrid test set have been developed. In this paper, we propose an improved estimation technique for fast generation of the hybrid test set.

The rest of the paper is organized as follows. In the following section an overview of the hybrid BIST is given. It is followed by a presentation of the hybrid BIST cost calculation in Section 3. Section 4 describes the proposed estimation methodology that is illustrated with experimental results in Section 5. The paper is concluded in Section 6.

2. Hybrid BIST

In general a hybrid BIST approach combines two different types of tests. It starts with a pseudorandom test sequence of length L and continues with some precomputed deterministic test patterns, stored in the system, in order to reach the desirable fault coverage. For off-line generation of the deterministic test

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patterns, arbitrary software test generators may be used, based on deterministic, random or genetic algorithms [3].

The length L of the pseudorandom test is an important parameter, which determines the behavior of the whole test process. A shorter pseudorandom test set implies a larger deterministic test set. This requires additional memory space, but at the same time, shortens the overall testing time. A longer pseudorandom test, on the other hand, will lead to longer test application time with reduced memory requirements. Therefore, it is crucial to determine the optimal length of pseudorandom test in order to minimize the total testing cost.

Figure 1 illustrates graphically the calculation of the total cost of a hybrid BIST solution consisting of pseudorandom test patterns and stored test patterns. We can define the total test cost of the hybrid BIST C_{TOTAL} as:

$$C_{TOTAL} = C_{GEN} + C_{MEM} = \alpha L + \beta S$$

where C_{GEN} is the cost related to the time for generating L pseudorandom test patterns (number of clock cycles), C_{MEM} is the memory cost for storing S precomputed test patterns (number of stored test patterns), and α, β are constants to map the test length and memory space to the costs of the two parts of the test solutions to be mixed.

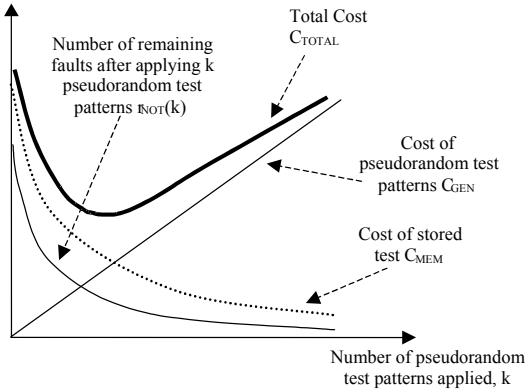

Figure 1. Cost calculation for hybrid BIST.

3. Cost Calculation for Hybrid BIST

The main purpose of this work is to propose a fast method for calculating the number of additional deterministic test patterns S for any arbitrary number of pseudorandom test patterns in order to reach the maximum obtainable fault coverage.

Creating the curve C_{GEN}, illustrated in Figure 1, is not difficult. For this purpose, a simulation of the behavior of the LSFR, used for pseudorandom test pattern generation, is needed. The fault simulation should be carried out for the complete test sequence generated by the LFSR. As a result of such a simulation, we find for each clock cycle the list of faults which are covered up to this clock cycle. By removing these faults from the complete fault list, we know the number of faults remaining to be tested.

More difficult is to find the values of βS, the cost for storing additional deterministic patterns in order to reach the given fault coverage level (100% in the ideal case). In [3] we proposed a method based on repetitive use of the ATPG and in [4] a method based on fault table manipulations was described. Both procedures are accurate but time-consuming and therefore not feasible for larger designs.

To overcome the complexity explosion problem we have developed an estimation technique that leads us to an approximate solution. This can be used as an initial solution for a search of more accurate results, using different optimization heuristics. In [5] a method based on Tabu search has been proposed.

The previously proposed estimation method was based on average information and was therefore not always very accurate [3]. In this previous work the analysis was performed based on the numbers of remaining faults for all efficient pseudorandom test patterns, and assumed based on some experimental evaluation that for ISCAS'85 benchmarks in average 1 remaining fault requires 0,45 deterministic test patterns to cover it. This information can be used to suggest a good point for starting a search for the global optimum by sampled calculation of the real cost function. It was demonstrated that the accuracy of this method is between 62% and 99%. In general, it is very difficult to find statistically a good approximation function general enough for different circuits.

In this paper we propose a new, improved method that is based on fault simulation results of the particular design and, as we will demonstrate with experimental results, has proven to be more accurate.

4. Test Cost Estimation Methodology

Let us denote the deterministic test set with *TD* and efficient pseudorandom test set [6] with *TPE*. In the following we will use *FD(i)* and *FPE(i)* to denote the fault coverage figures of the test sequences *TD*(*i*) and *TPE*(*i*), correspondingly, where *i* is the length of the test sequence.

Procedure 1: Estimation of the length of the deterministic test set TD.

1. Calculate, by fault simulation, the fault coverage functions $FD(i)$, $i = 1, 2, \ldots, |TD|$, and $FPE(i)$, $i = 1, 2, \ldots, |TPE|$. The patterns in *TD* are ordered in such the way that each pattern put into the sequence contributes with maximum increase in fault coverage.
2. For each $i^* \le |TPE|$, find the fault coverage value F^* that can be reached by a sequence of patterns $(P_1, P_2, \ldots, P_{i^*}) \subseteq TPE$ (see Figure 2).
3. By solving the equation $FD(i) = F^*$, find the maximum integer value j^* that satisfies the condition $FD(j^*) \le F^*$. The value of j^* is the length of the deterministic sequence that can achieve the same fault coverage F^*.
4. Calculate the value of $|TD^E(i^*)| = |TD| - j^*$ which is the number of test patterns needed from the *TD* to reach to the maximum achievable fault coverage.

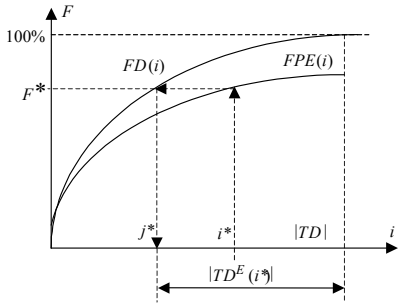

Figure 2. Estimation of the length of the deterministic test sequence.

The value $|TD^E(i^*)|=|TD|-j^*$, calculated by the Procedure 1, can be used to estimate the length of the deterministic test sequence TD^* in the hybrid test set $TH = \{TP^*, TD^*\}$ with i^* efficient test patterns in TP^*.

By finding $|TD^E(j)|$ for all $j = 1, 2, \ldots, |TPE|$ we get the cost function estimate $C^E_{MEM}(j)$.

In the following we will illustrate the procedure 1 with an example. In Figure 3 we have presented an extract of the fault simulation results for both test sets. The length of the pseudorandom sequence has to be only so long as potentially necessary. By knowing the length of the complete deterministic test set and fault coverage figures for every individual pattern we can estimate the size of the additional deterministic test set for any length of the pseudorandom test sequence, as illustrated in the Figure 3. Here we can see that for a given core 60 deterministic test cycles are needed to obtain the same fault coverage as 524 pseudorandom test cycles and it requires additional 30 deterministic test cycles to reach 100% fault coverage. Based on this information we assume, that if we will apply those 30 deterministic test cycles on top of the 524 pseudorandom cycles, we can obtain close to the maximum fault coverage.

|TP|	*FC%*	*|TD|*	*FC%*
1	21.9	1	43.3
2	34.7	2	45.6
	…		
524	97.5	60	97.5
	…		
1000	98.9	90	100

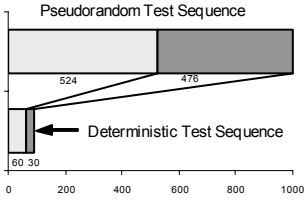

Figure 3. Estimation of the length of the deterministic test sequence.

5. Experimental Results

We have performed experiments with all designs from the ISCAS85 benchmark family. Some of those results are illustrated in Figure 4. In those charts we have depicted the memory requirement (the size of the deterministic test set) for every pseudorandom test length. Obviously – the longer the pseudorandom test

sequence is, the smaller is the memory requirement. We have compared our earlier estimation methodology [3] against the estimation methodology proposed in this paper. In addition, we have also depicted the real memory cost. This has been obtained by the repetitive use of ATPG [3]. As it can be seen from the results, our new estimation methodology gives better estimates than the previous one (the curve "New Approximate" is much closer to the "Real" than the "Old Approximate"), mainly in the situations, when the hybrid test set contains smaller amount of pseudorandom test patterns.

This approximation methodology can be used in different contexts. It can be used for total test cot minimization for single-core designs (as described in [3], [4], [5]). We have also demonstrated that the same estimation methodology can be used efficiently for test time minimization for multi-core designs, under tester memory constraints. The method has been proved efficient with combinatorial cores [6] as well as with sequential cores [7].

6. Conclusions

In this paper we have proposed an improved estimation technique that can be used for hybrid BIST test set generation. The exact method for finding the optimal hybrid test set configuration is computationally expensive and therefore a fast estimation procedure is highly useful, especially for large designs.

As it was shown by the experiments, the improved estimation algorithm has produced significantly better results than the estimation method used earlier. It can also be used as a better starting point for the search for the global optimal solutions.

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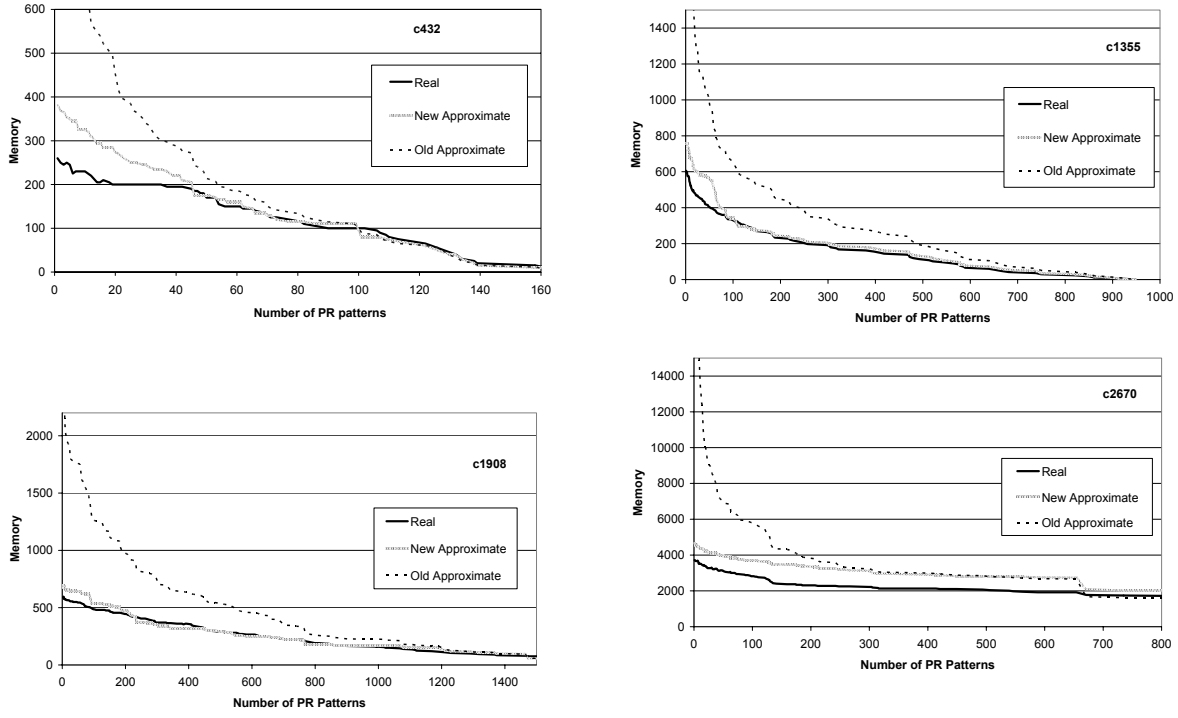

Figure 4. Experimental results with ISCAS 85 benchmark designs.