COTEST/D5

Report on Dissemination Plan

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Related documents

- COTEST Technical Annex
- COTEST Report D1: Report on benchmark identification and planning of experiments to be performed
- COTEST Report D2: Report on Automatic Generation of Testbenches from System-level Descriptions
- COTEST Report D3: Report on Early DfT Support
- COTEST Report D4: Final Report on Project Results

1. Introduction

The COTEST project aimed at assessing whether it is feasible and effective to take test issues into account early in the digital system design process, when only a behavioral description of the designed system is available. The project focused on two main problems: generation of test sequences starting from behavioral descriptions and modification of behavioral descriptions to increase testability (Design for Testability).

Due to the critical nature of this assessment project, it is extremely important to obtain as much feedback about the results as possible. The results have been discussed on meetings with industry, academic partners and in the framework of several other Community projects. Several scientific papers have been published or submitted for publication. In the following the current dissemination status and future dissemination plans of both partners will be given.

2. Politecnico di Torino

2.1. Publications

- Published paper:

  O. Goloubeva, M. Sonza Reorda, M. Violante, "Experimental analysis of fault models for behavioral-level test generation," IEEE DDECS2002: Design & Diagnostic of Electronic Circuits & Systems, 2002, pp. 416-419

- Accepted paper:

  O. Goloubeva, M. Sonza Reorda, M. Violante, "Behavioral-level fault models comparison: an experimental approach," ICAM2002, Computer-aided Technologies in Applied Mathematics, September 2002, Tomsk, Russia

- Submitted paper:

  O. Goloubeva, M. Sonza Reorda, M. Violante, "Behavioral-level test vector generation: fault model selection and preliminary test generation results", *17th Conference on Design of Circuits and Integrated Systems (DCIS 2002)*, DCIS 2002, Spain, November 2002

2.2. Meetings with Industry and other Universities

The project was presented and discussed during several meetings with representatives from the following industries and universities:

- Centro Ricerche Fiat (Torino, Italy)

- ST microelectronics (Milano, Italy)
- GeTeDef (Grenoble, France)
- Technical University of Brandenburg (Cottbus, Germany)
- Università di Napoli II (Napoli, Italy).

The project activities and results have also been presented in the meetings of the ISIDE project (*Sviluppo di sistemi di elaborazione reattivi ed affidabili per applicazioni industriali*) funded by the Italian Ministry for Education, Research and University.

2.3. Contacts with other Community projects

The results will also be exploited in an already planned seminar to be given to the partners of the ALFA program TOSCA project (*Fault-Tolerant System Design and Verification for Safety-Critical Applications*), which is supported by the European Commission for the cooperation between European and Latin American universities.

2.4. Training

The results of the project will be exploited in the Computer Science curricula at PdT, e.g., within the course “Design techniques for reliable circuits”, for PhD students.

3. Linköping University

3.1. Publications

- Abdil Rashid Mohamed, Zebo Peng, Petru Eles, “BIST Synthesis: An Approach to Resources Optimization Test Time Constraints”, *5th Design and Diagnostic of Electronic Circuits and Systems (DDECS2002)*, pp. 346-351, Czech Republic, 2002.
- Gert Jervan, Zebo Peng, Raimund Ubar, Helena Kruus, “A Hybrid BIST Architecture and its Optimization for SoC Testing”, *IEEE 2002 3rd International Symposium on Quality Electronic Design (ISQED'02)*, pp. 273-279, USA, 2002.
- Raimund Ubar, Helena Kruus, Gert Jervan, Zebo Peng, “Using Tabu Search Method for Optimizing the Cost of Hybrid BIST”, *16th Conference on Design of Circuits and Integrated Systems (DCIS 2001)*, pp. 445-450, Portugal, 2001.
- Raimund Ubar, Gert Jervan, Zebo Peng, Elmet Orasson, Rein Raidma, “Fast Test Cost Calculation for Hybrid BIST in Digital Systems” *Euromicro Symposium on Digital Systems Design*, pp. 318-325, Poland, 2001.

3.2. Meetings with Industry and other Universities

Results of the project were presented and thoroughly discussed on regular Swedish Network of Design for Test (www.sndft.org) meetings. SNDFT is a collection of researchers from Swedish universities and industries who try to address and solve testing problems of modern complex electronic systems.

Several issues related to the COTEST project have also been presented at INTELECT meetings and workshops. INTELECT is a Swedish national research program financed by the Swedish Foundation for Strategic Research (SSF) with an objective to put Swedish academic institutions in the international forefront in the field of integrated electronic systems.

The results were also presented in the framework of Swedish Socware initiative (www.socware.com) and discussed on meetings with industrial and academic partners.

Meetings with representatives from following companies were carried out:

- Ericsson's CadLab Research Center
- Ericsson Radio Systems AB
- Saab Dynamics AB
- Spirea AB

3.3. Training

The concepts and results from the project have been successfully introduced to several course materials, which are used for industrial as well as academic training:

- Testing of Digital Systems – graduate course at Linköping University
- System Level Synthesis with VHDL – industrial course coordinated by Acreo AB
- Computer Aided Design of Electronics – undergraduate course at Linköping University

Several results of the project will also be integrated into a course in the test area to be given in the EU project on System Design Industry Council Training (IST 2001-35100).

3.4. Contacts with other Community projects

LiU has been participating in several Community financed projects. Significant amount of new ideas have risen from the synergy generated by the VILAB project (INCO-Copernicus project 977133) and the results of the COTEST project have been relayed back to the participating institutions. In the future COTEST results will be exploited by the SYDIC-TRAINING project (IST 2001-35100), which will provide training on advanced system specification and validation methods of electronics systems.

4. COTEST Website

The COTEST website was set up at the beginning of the project and maintained continuously by LiU. It includes project overview, history of meetings together with slides, results as well as publications.

- www.ida.liu.se/~eslab/cotest.html