Test Cost Modeling for 3D Stacked Chips with Through-Silicon Vias

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Abstract—In this paper we have proposed a test cost model for core-based 3D Stacked ICs (SICs) connected by Through Silicon Vias (TSVs). Unlike in the case of non-stacked chips, where the test flow is well defined by applying the same test schedule both at wafer sort and at package test, the most cost-efficient test flow for 3D TSV-SICs is yet undefined. Therefore, analysing the various alternatives of test flow, we present a cost model with the optimal test flow. In the test flow alternatives, we analyse the effect of all possible moments of testing for a 3D TSV-SIC, *viz.,* wafer sort, intermediate test and package test. For the optimal test flow, we have performed experiments with various varying yield and test time parameters, which further support our claim.

I. INTRODUCTION

Integrated circuits (ICs) with multiple chips (dies) stacked and bonded vertically, interconnected with Through-Silicon Vias (TSVs), so called 3D TSV Stacked ICs (TSV-SICs), have lately attracted a fair amount of research [1]–[5]. Recent research have addressed test architecture design for 3D TSV-SICs [6], testing the TSVs [1]–[6] and 3D TSV-SIC specific defects [1], [2]. Due to imperfections in IC manufacturing, traditionally, each individual chip was tested twice [7], [8] in the following instances:

1) Wafer sort: Since IC packaging is costly [9], in this stage, the bare chip is tested, to avoid packaging of faulty chips. The chips which appear to be fault free during wafer sort are termed Known Good Dies (KGDs).
2) Package test: KGDs are packaged, and the test is applied to the complete packaged IC.

For non-stacked ICs the same test schedule is applied to both the bare chip and the packaged chip. However, for a 3D TSV-SIC the package test includes the test schedules for all the chips forming the stack after each chip has been tested in wafer sort. As will be illustrated in this paper, applying the optimized test schedule used for the individual chips during wafer sort to the stack of chips during package test for a 3D TSV-SIC may lead to sub-optimal test application time (TAT). Here, TAT is defined as the sum of the testing times for wafer sort and package tests. It should be noted that TAT is a major part of the overall test cost [8]. Hence, it is important to schedule the tests for 3D TSV-SIC so that TAT is minimized, which is addressed in this paper.

As mentioned above, the fact that tests are to be performed at both wafer sort and package test affects test scheduling. In contrast to the traditional test of non-stacked chips, where

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wafer sort and package test could be the same, the package test of a 3D TSV-SIC includes testing all cores of all chips in the stack, along with the TSVs. Performing tests on all cores concurrently would consume a lot of power and risk false positives from voltage-drop and damage due to over-heating. On the other hand, performing the same test schedules as in wafer sort in package test but over one chip at a time would take an unnecessarily long time, as will be shown in this paper. Therefore, we propose a power constrained test scheduling approach for 3D TSV-SICs.

This paper proceeds with related in Section II, followed by background on the manufacturing and testing process of 3D TSV-SICs in Section III. A cost model, analyzing the various possible test schemes for 3D TSV-SICs, is described in Section IV. The experimental results are shown in Section V and the conclusions are in Section VI.

II. RELATED WORK

In [11], a test cost analysis has been performed for 3D TSV-SICs, with upto six chips in a packaged stack. The yield of each die is assumed to be within a range of 60% to 90%, while the stack yield and TSV yield are assumed to be constant, 93% and 99%, throughout the paper. [11] compares the test flow of non-stacked ICs with 3D TSV-SICs. Case studies show that including wafer sort in the test flow results in reduction of the overall chip cost. In addition, it is concluded that fewer number of tests may not reduce the overall 3D TSV-SIC cost and the test cost and cost loss also depends on the test yields of the intermediate partial stacks and the final stack before and after packaging.

In Section IV, we perform a test cost analysis for 3D TSV-SICs to arrive at an economic test scheme for 3D TSV-SICs. Different from [18] who makes their analysis for chip yield values in the range of 60% - 90%, a constant stacked yield of 93%, and a constant TSV yield of 99%, our analysis includes any yield values for chips and TSVs and reasonable yield values (> 0.9) of the stacked chips. Also, our cost analysis shows that a test flow testing partial stacks leads to higher test cost. We perform the analysis over a range of yield values shown in Table I. Although, we describe the test schemes using a specific set of values, thus arriving at the conclusion to perform the package test on the stacked and packaged KGDs obtained after wafer sort.

III. BACKGROUND

To continue according to Moore's law, having more functionality into smaller form factors, reducing power and cost

while enhancing the performance, integrated circuits (ICs) with multiple chips (dies), called 3D TSV-SICs have been developed. Earlier versions of high integration in non-stacked multiple chip ICs include:

- Printed Circuit Boards (PCBs), with multiple ICs on the same board
- System-on-Chip (SoC), with multiple cores in a chip
- Multi-Chip-Package (MCP), where multiple dies are integrated in a single package [1].

Eventually multi-chip ICs were stacked vertically, but not bonded with TSV interconnects, or elevators, which include:

- System-in-Package (SiP), where dies are vertically stacked within a package, interconnected by wire-bonds to the substrate
- Package-on-Package (PoP), where multiple chips are vertically stacked

Although 3D TSV-SICs has its advantages in terms of performance or power requirements, the manufacturing process introduces new challenges in terms of achieving high yield, testing and power constraints [1], [2].

Since 3D TSV-SICs are unlike any other ICs due to the presence of TSVs, also known as elevators, among the layers of the stack, the manufacturing process for 3D TSV-SICs is different. 3D TSV-SICs can be obtained by three stacking processes, viz, Die-to-Die (D2D), Wafer-to-Wafer (W2W) and Die-to-Wafer (D2W). In W2W stacking, complete wafers are stacked over one another, resulting in exponentially decreasing yields with increasing number of layers in the stack [6]. Therefore, this paper considers D2W and D2D stacking [6].

While stacking, the orientation of the stacked chips has to be considered. There are three possible variations in this regard: face-to-face, back-to-back and face-to-back. In this context, the face of a chip is the side of the transistors and the metal interconnect layers and the back is the silicon substrate layer. Among the three possibilities, only face-to-back bonding is scalable to stacks of more than two chips [1]. Hence, only face-to-back bonding is applicable for this paper.

The test flow model as discussed in [1] is shown in Fig. 1.

A traditional non-stacked chip is tested twice at the two levels (Fig. 1(a)), viz. (i) wafer sort and (ii) package test. Wafer sort is motivated by the fact that packaging the faulty products is more expensive than the test itself. By testing, unnecessary packing of faulty chips is avoided. For non-stacked chips, the only possible introduction of faults after wafer sort might occur while packaging the same IC. Therefore, the test performed at wafer sort is repeated at the package test.

In case of 3D TSV-SIC, as seen in Fig. 1(b), there are four steps in the stacking process when faults can be introduced to any individual chip of the stack: (i) die fabrication, (ii) when the bottom of the chip is bonded to the stack, (iii) when another chip is bonded to the top of the chip, (iv) packaging. Based on these steps, several test runs can be considered, one for each step that can introduce faults. For a three-chip stack, these test runs can be referred to as wafer sort, test after the first stacking event (for the two chips that are first stacked together), test after the second stacking event and package test, as shown in Fig. 1(b). It should be noted that testing after a stacking event or package test includes testing the TSVs.
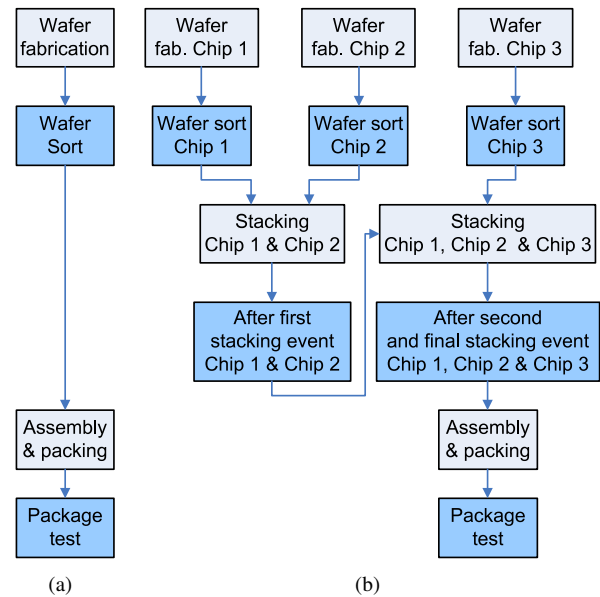

Fig. 1.   (a) 2D test flow [1], (b) 3D test flow (for 3D TSV-SICs) [1]

Chip-specific test schedules that are optimized for wafer sort do not consider testing of other chips in the stack. Similarly, test schedules that are optimized for the package test are not necessarily optimal for wafer sort. Thus, it can be seen that a complete view of test scheduling from wafer sort through to package test is required in order to arrive at a minimal TAT.

IV. Cost model

A major part of the chip cost accounts for the testing of the chips [1]. In the example of Fig. 1(b), it can be seen that stacking three chips to make a 3D TSV-SIC can lead to testing the same chip four times. That is twice the test cost per chip, as compared to traditional non-stacked testing.

To arrive at an efficient low-cost test scheme, we develop a cost model considering the test flow graph in [1]. In [11], Taouil *et al.* defined and employed a detailed cost model for testing 3D TSV-SICs to conclude that inclusion of wafer sort in the test flow results in reduction of the overall cost. Furthermore, they observed benefits from TSV tests in partial stacks. For various parametrs of the schemes mentioned below, we arrive at the most cost-efficient test scheme:

- A: Wafer sort test followed by testing the TSVs after each stacking event, and package test
  In Fig. 1(b), the second level of events from the top implemented; in the fourth level, only TSV tests are performed and then the lowermost level, package test is performed.
- B: Complete stack test after all stacking events, and package test
  Only the rightmost event of the fourth level from the top, and the package test, in Fig. 1(b) are implemented.
- C: Wafer sort followed by partial stack tests after each stacking event, and package test
  Here all the events in the second, fourth and sixth levels from the top in Fig. 1(b) are performed. All chips of the

stack are tested in each event, and the TSVs are tested in all stages, but the topmost one.

In contrast to [11], we assume that the tests are perfect in the sense that all faults are correctly detected. The parameters of our cost model are: The manufacturing yield Y_C and the test time T_C for each chip C. Similarly, the test yield and test times for TSV testing are Y_{TSV} and T_{TSV} respectively. We assume each stacking step and packaging may damage the chip, with the yield Y_D.

We illustrate our cost model with an example of a three chip 3D TSV-SIC, where the test times and yield values for each component are shown in Table I. In this table we arrive at 100 good packaged chips applying the three mentioned schemes A, B and C. The total time spent in testing all the components that result in 100 good packaged chips is calculated. The cost is related to the required number of chips to arrive at 100 good packaged chips.

For each step in the test scheme (wafer sort, after first stacking event, after second stacking event, package test) we calculate the test time which depends on the number of stacked components to test. Furthermore, we calculate the time spent testing faulty components and components that end in a faulty stack, which we term as waste.

The number of components to be tested in a given step is calculated using Equation 1.

$$Quantity = \frac{\text{Desired output quantity}}{\prod Y_{\text{untested components and steps}}} \quad (1)$$

Equation 1 expresses that in order to manufacture 100 good packaged 3D TSV-SICs, it may be necessary to test more than 100 components, due to yield loss. This yield corresponds to the components that are yet untested and the yield of subsequent stacking steps.

The time taken to test the given number of components is as Equation 2:

$$TestTime = \sum_{\text{tested components}} (Quantity \cdot T_C) \quad (2)$$

For a given step in the test scheme, where a number of components are tested for the first time, the time spent in testing faulty components or components that end up in a faulty stack is given by Equation 3:

$$Waste = Quantity \cdot \quad (3)$$
$$\cdot \left(\sum \text{Test time for stacked components} \right) \cdot$$
$$\cdot \left(1 - \prod Y_{\text{components tested for the first time}} \right)$$

With Equation 1, Equation 2 and Equation 3, it is possible to express the following: To get N good packaged chips, where the chip design has yield Y_C and takes T_C time units, while the package has yield Y_p and takes T_p time units, it may be necessary to test $\frac{N}{Y_C \cdot Y_p}$ chips in wafer sort and $\frac{N}{Y_p}$ packaged chips in package test. Thus, wafer sort will take $T_C \cdot \frac{N}{Y_C \cdot Y_p}$ time units and package test will take

TABLE I
TEST COST FOR INDIVIDUAL PARTS OF 3D TSV-SIC

Component	Test Time	Yield
Chip 1	3000 t.u.	0.9
Chip 2	20000 t.u.	0.92
Chip 3	100000 t.u.	0.87
TSV	500 t.u.	0.95
Package	500 t.u.	0.95
Yield per stacking step	0.95	

$(T_p + T_C) \cdot \frac{N}{Y_p}$ time units. The waste (time spent testing faulty chips or faulty packages) amounts to $(1 - Y_C) \cdot \frac{N}{Y_C \cdot Y_p} \cdot T_C$ and $(1 - Y_p) \cdot \frac{N}{Y_p} \cdot (2 \cdot T_C + T_p)$ for wafer sort and package tests respectively. It should be noted that T_C is counted twice in the calculation of the waste from the package test, because at that point, the chips are tested for the second time.

V. EXPERIMENTAL RESULTS

In his section we analyse the three test schemes menioned in Section IV, with varying yield and test time values. A particular example has been discussed below in detail.

In Table I, from the left, the first column lists the components to be tested. It should be noted that there are two instances of TSVs in the stack, between Chip 1 and Chip 2, and between Chip 2 and Chip 3. The second and third columns show the test time required and the respective yield values for each component. The final row of Table I shows the yield of a stacking step. Here, we use 0.95 yield to express that when Chip 2 is stacked upon Chip 1, five out of a hundred partial stacks are damaged. Similarly when Chip 3 is stacked on top of Chip 1 and Chip 2. Also for packaging, it is assumed that five out of a hundred stacks are damaged.

The example of the cost model is carried through in Table II. The four testing events, *viz.*, wafer sort, after first stacking event, after second stacking event and package test are analyzed. In a group of four sub-columns for each testing event, listed are the components that are tested (chips and/or TSVs), the total number of components tested under quantity, the total time taken for the testing event as test time and waste is the time spent on testing products that do not pass the testing event.

For test scheme A, 133 Chip 1, 131 Chip 2 and 138 Chip 3 are tested in wafer sort to obtain KGDs. The sum 402 is given in column 3. Wafer sort takes in total 16819000 time units as in column 4. Because of the yield of the three chips, 2043500 time units are wasted on faulty chips as detailed in column 5. Wafer sort results in 120 good chips of each type. That means that 120 partial stacks of Chip 1 and Chip 2 are manufactured and testing the TSVs in the partial stacks takes 60000 time units. From this test it is revealed that 143850 time units are wasted on testing components that will never be a part of a 3D TSV-SIC. The process goes on in test scheme A where 113 good partial stacks, consisting of Chip 1 and Chip 2, are combined with Chip 3 and another TSV test is applied, after the second stacking event. Before the package test, there are 106 stacks, which because of the yield of packaging and the risk of damage end up as 100 good 3D TSV-SICs. Similar observations can be made about test scheme B and test scheme

TABLE II
TEST SCHEMES

Scheme	Wafer sort				After first stacking event			
	Components	Quantity	Test time	Waste	Components	Quantity	Test time	Waste
A	Chips 1,2&3	402	16819000	2043500	TSV layer 1-2	120	60000	143850
B	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
C	Chips 1,2&3	402	16819000	2043500	Chips 1&2, TSV 1-2	120	2820000	412950

Scheme	After second stacking event				Package test				Total		
	Components	Quantity	Test time	Waste	Components	Quantity	Test time	Waste	Quantity	Test time	Waste
A	TSV layer 2-3	113	56500	703284	All	106	13197000	1317050	100	30132500	4207684
B	Chips 1,2&3, TSV 1-2,2-3	166	20584000	8506590	All	106	13197000	1317050	100	33864000	9823640
C	Chips 2&3, TSV 2-3	113	13616500	2155334	All	106	13197000	2074950	100	46452500	6686734

C. In particular, test scheme B, which tests the chips of the stack for the first time, after all the chips have been stacked, requires 166 chips of each type to ensure that there will be 100 good TSV-SICs. Our conclusion from the cost model is that test scheme A has the lowest cost in terms of test time and the number of required chips. Furthermore, test scheme A spends the least amount of time on testing components that will not be used in a good 3D TSV-SIC.

Similar applications of the cost model as in the example above has been repeated for various yield and test time values. We have seen that the observations made regarding the benefits of test scheme A hold for reasonable yield values (> 0.9).

VI. CONCLUSION

From the above analysis of various test cost schemes, it can be concluded that scheme A is the most economic in terms of test time and waste. Therefore, for the rest of the paper we will assume scheme A, *i.e.*, two steps in the test flow: wafer sort (each individual chip), followed by packaging (complete packaged stack).

Hence, it can be concluded that, test flows including wafer sort results in significant reduction of the overall test cost. A cost-efficient test flow scheme, such as scheme B, does not necessary results in lower overall 3D TSV-SIC cost. The most cost-effective test flow consists of wafer sort and strongly depends on the stack yield. This requires the adaptation of the test flow during the yield learning of the 3D TSV-SIC manufacturing process. Moreover, test architectures should provide access to all dies as well as all interconnects of the SIC in order to be able to perform intermediate tests.

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