Test Scheduling and Test Access Optimization for Core-Based 3D Stacked ICs with Through-Silicon Vias

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In the race against Moores Law, integrated chips (ICs) with multiple dies stacked over one another and connected by Through-Silicon Vias (TSVs), called 3D TSV-Stacked ICs (SICs) have attracted a fair amount of research [1]–[5]. Due to imperfections in IC manufacturing, each individual chip must be tested. Testing each IC, increases cost, which is highly related to the testing time spent on each IC. Test scheduling approaches, aiming at minimizing testing times, for non-stacked ICs have been discussed in [6]–[8]. Although no work has yet been visible for scheduling tests under power constraints for 3D TSV-SICs. Applying traditional test scheduling methods used for non-stacked chip testing, where the same schedule is applied both at wafer sort and package test, to 3D TSV-SICs, leads to unnecessarily high TAT. This is because in case of 3D TSV-SICs, the package test involves testing of all the chips in the stack together. Therefore, tests scheduled for individual chips during wafer sort using [6], [7] do not perform well during package test. A key challenge in 3D TSV-SIC testing is to reduce TAT by co-optimizing wafer sort and the package test.

In our work, we consider a system of chips with cores that are accessed through an on-chip JTAG infrastructure, based on [9], [10] and shown in Fig. 1, and we propose a test scheduling approach to reduce TAT while considering resource conflicts. Fig. 1 illustrates the scan chains that start from a JTAG TAP, proceeds through one or more cores and returns back to the JTAG TAP. It should be noted that, only one scan chain can be accessed at a time. Thus, if tests for more than one core of a chip are to run concurrently, in a session, these cores are connected in series on the JTAG interface, forming a single scan chain. This enforces the concept of sessions as introduced in [6]–[8]. For a single chip, only cores that are in the same scan chain can be tested concurrently. Furthermore, if two cores are to be tested in sequence, in different sessions, they cannot be connected in the same scan chain. On the other hand, a session of tests from a chip can be performed concurrently with a session of tests from another chip by selecting the scan chains in the TAPs of to the two chips.

For any core, say Core3 in Fig. 1, the test time (T_3) required can be calculated as a function of the length of the scan chain of Core3 (l_3) and the number of patterns required (p_3):

$$\begin{aligned} T_3 &= (l_3+1)\cdot p_3 + (l_3+1) \\ &= (l_3+1)\cdot(p_3+1) \\ &= L_3 \cdot P_3 \end{aligned}$$

Where, $L_3 = (l_3+1)$ and $P_3 = (p_3+1)$

On the other hand, the total time taken by the scan chain including both Core1 and Core2 is given as the product of the sum of the lengths of the individual scan chains of Core1 and Core2 with the maximum number of pattern counts among Core1 and Core2, as can be seen below:

$T_{1+2} = max.(P_1, P_2)\cdot(L_1+L_2)$

It should be noted that the hardware cost increases with increasing number of scan chains (or sessions). On the other hand, combining the scan chains of two cores having unequal number of pattern counts, results in increase of the total test time, as illustrated in the example that follows.

Table I lists the L and P values for each core of the 2-chip 3D TSV-SIC illustrated in Fig 1. We calculate the total test time for wafer sort (ws) and package test (pt) for the configuration shown, i.e., Core1 and Core2 with a common scan chain, forming session 1 (S_1), Core3 forming session 2 (S_2), Core4 session 3 (S_3) and Core5 session 4 (S_4):

$$\begin{aligned} T_{ws} &= T_{1+2} + T_3 + T_4 + T_5 \\ &= max.(P_1,P_2)\cdot(L_1+L_2) + L_3\cdot P_3 + max.(P_4,P_5)\cdot(L_4+L_5) \\ &= 50\cdot 90 + 30\cdot 30 + 20\cdot 30 = 6000\ time\ units\ (t.u.) \end{aligned}$$

Performing the tests in the same order on package test as in wafer sort would result in

$T_{ws} = T_{pt}$

Therefore the total test time becomes,

$T = T_{ws} + T_{pt} = 6000 + 6000 = 12000\ t.u.$

Similarly, considering separate scan chains for all five cores would give, $T = 11000\ t.u.$ But as a trade-off, it results in more number of sessions, thus an increased hardware cost.

The minimum number of sessions is obtained when during wafer sort Core1, Core2 and Core3 are in S_1 and Core4 and Core5 are in S_2, while during package test all five cores are in the same session. The total time leads to $T = 14100\ t.u.$, which is much higher than the alternative distribution of sessions discussed above, although, in this case, the hardware requirement is minimum.

A trade-off between the alternatives mentioned above is to have two sessions during both wafer sort and package test, with Core1, Core2 and Core3 in S_1 and Core4 and Core5 in S_2. Then the total time sums up to, $T = 13200\ t.u$, as seen in Table II.

But, on the other hand, if the test of Core3 is performed along with Core4 and Core5, instead of Core1 and Core2, we find, in Table II, that the total test time reduces to $T = 12300\ t.u.$ It must be noted here that this alternative demands lesser number of sessions as the first alternative where the five cores were tested in five different sessions during both wafer sort and final test, while requires lower test time as compared to the alternative where all cores of a chip are tested in the same session during wafer sort and there is only one session during package test.

Therefore, from the above studies on the distribution of scan chain in a 3D TSV-SIC it was seen that the test time can be reduced by increasing the number of scan chains, thereby increasing the number of sessions. Although, an increased number of sessions imply increased hardware cost. Hence, a trade-off between the hardware cost and the test time can be obtained in order to give the minimum total effective cost in terms of hardware cost and test time.

TABLE II
TEST SESSION ALTERNATIVES (WITH ALTERNATIVE 2 AS BASELINE)

Alternative	**Wafer Sort** (ws) **Chip 1** Core Tests in Sessions	Time	**Chip 2** Cores Test in Sessions	Time	**Package Test** (pt) Cores Test in Sessions	Time	**Total Time** $t.u.$ (% incr.) $T_{ws} + T_{pt}$	**No. of Sessions** orig (% decr)
1	(1, 2) + (3)	5400	(4, 5)	600	(1, 2) + (3) + (4) + (5)	6000	12000 (9)	8 (20)
2	(1) + (2) + (3)	5000	(4) + (5)	500	(1) + (2) + (3) + (4) + (5)	5500	11000 (0)	10 (0)
3	(1, 2, 3)	6000	(4, 5)	600	(1, 2) + (3) + (4) + (5)	7500	14100 (28)	3 (70)
4	(1, 2, 3)	6000	(4, 5)	600	(1, 2) + (3) + (4, 5)	6600	13200 (20)	4 (60)
5	(1, 2) + (3)	5400	(4, 5)	600	(1, 2) + (3, 4, 5)	6000	12300 (12)	5 (50)

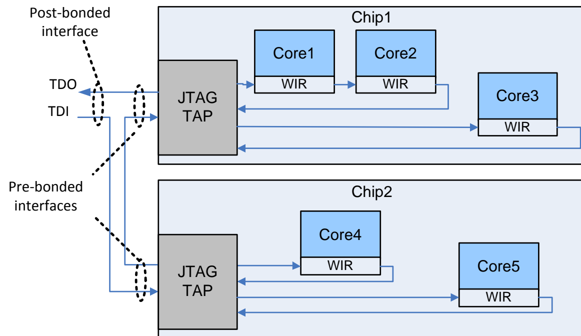

Fig. 1. Test architecture of 3D TSV-SIC with JTAG

TABLE I
GIVEN L, P VALUES FOR EACH CORE OF THE 3D TSV-SIC

	Chip 1 **Core1**	**Core2**	**Core3**	**Chip 2** **Core4**	**Core5**
L	50	40	30	20	10
P	50	40	30	20	10

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