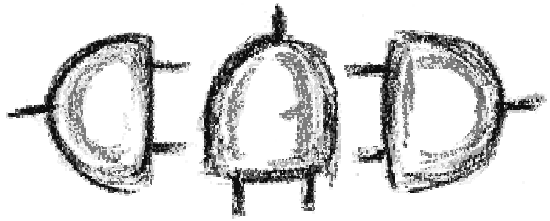
Politecnico di Torino
Dipartimento Automatica e Informatica
Torino, Italy

Electronic CAD & Reliability Group



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The Group

- **3 Faculty Members**
- **2 Research Assistants**
- **1 PhD students**
- **1 Full-time Graduate Developer**
- **~ 10 thesis students/year**
- **Year 2000 Income from Contracts: >200.000 Euros**
- **In the last 3 years:**
  - **7 papers in international journals and magazines**
  - **about 50 papers at major conferences**

Areas of Interest

- **ASIC and System Test**
  - **High-level ATPG and DfT**
  - **BIST**
  - **Test of Low-Power Circuits**
- **Reliability and Fault Tolerance**
- **Design Validation.**

On-going Cooperations

- **Industries:**
  - **STMicroelectronics, Milano**
  - **Italtel, Milano**
  - **Centro Ricerche FIAT, Torino**
  - **Elcis, Torino**
  - **NEC USA, Princeton**
- **Universities and Research Centers:**
  - **Brandenburg Technical University, Cottbus, Germany**
  - **TIMA, Grenoble, France**
  - **University Carlos III, Madrid, Spain.**

On-going Projects

- **UE: *Amatista* (with Alcatel Espacio, Madrid; UCIII, Madrid; CRF, Torino; FTL, Southampton):**
  - **Tools for VHDL Fault Tolerant structures Insertion and Fault Injection.**
- **ASI (*Italian Space Agency*)**
  - **Software Fault-Tolerance**
  - **Fast Fault Injection techniques**
- **Italian Ministry for University:**
  - **Tools for Fault Tolerant systems design.**

Current Research Activities

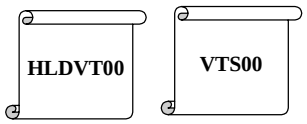
- **Testing**
- **Design Validation**
- **Fault Tolerance.**

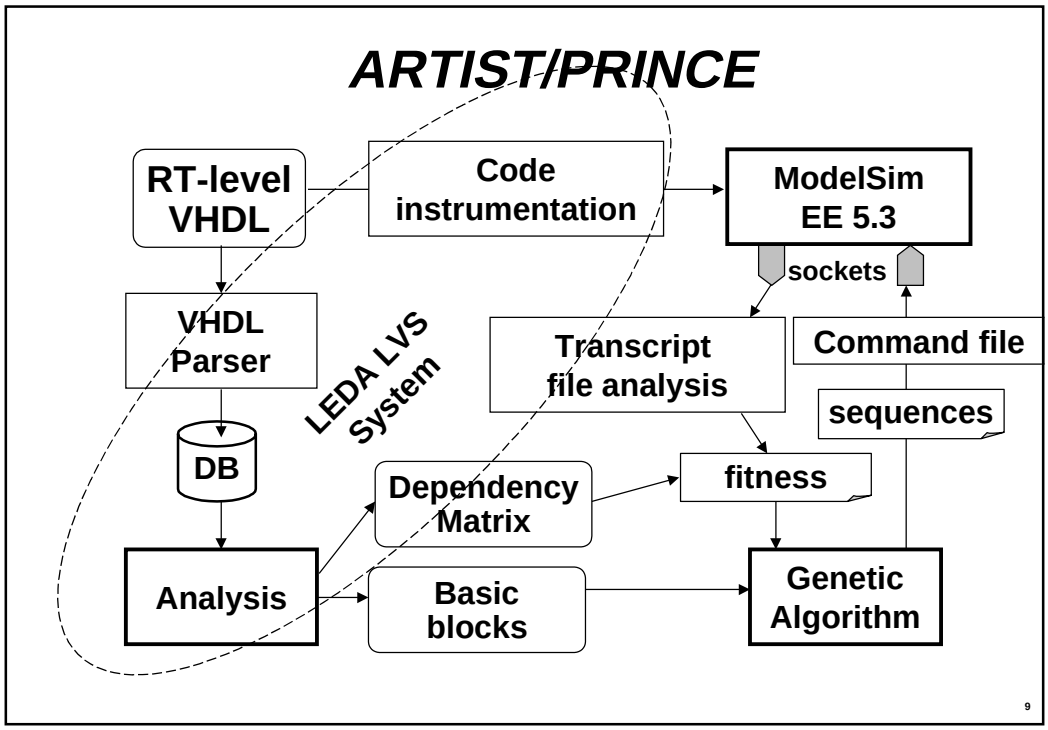
Testing

- High-level ATPG
- Processor Testing
- BIST
- Test for Low-Power Circuits
- Test and Co-design.

High-level ATPG

- Test pattern generation from RT-level or behavioral-level descriptions
- Generated patterns can be exploited at gate-level or used as an early testability indicator
- High-level fault model: RT-level assignment single-bit stuck-at
- Strategy: genetic algorithm + commercial simulator.





Benchmark Development

The group provided a subset of the ITC'99 benchmark circuits:

- **suitable for high-level ATPG evaluation**
- **RT-level VHDL descriptions**
- **synthesized gate-level netlists**
- **fault lists.**

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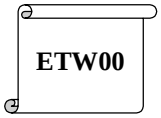
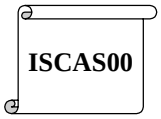
Processor testing

- **At-speed testing via execution of test program**
- **Test program generation in two phases:**
  - **Library of test macros**
  - **Optimization algorithm to tune macro parameters**
- **Experiments on Intel 8051.**

BIST

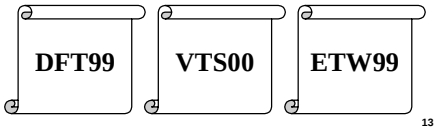
- **CA-based BIST for**
  - **pseudo-random testing**
  - **deterministic testing**
  - **improved CSTP.**





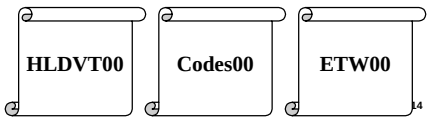
Low-power testing

- During test phases low-power circuits can dissipate much more than during normal behavior
- Possible troubles can arise in terms of circuit reliability and even destruction
- Solutions:
  - new ATPG algorithms
  - new BIST structures
  - suitable test plan.



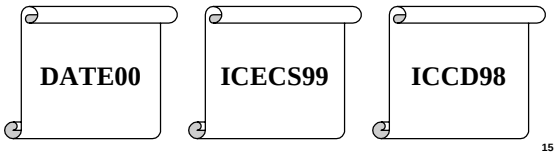
Test and Co-Design

- Goal: providing the designer with testability-oriented features in a co-design environment
- Advantages:
  - early testability evaluation
  - automatic DfT structures insertion
  - test plan optimization
  - automatic test bench generation
- Adopted co-design environment: POLIS.



Design Validation

- Approximate equivalence verification
- Approximate Model Checking
- Automatic Test Bench Generation for Design Validation.



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Design for Fault Tolerance

- Fault Injection:
  - Required to
    - Debug Fault Tolerant mechanisms
    - Evaluate the circuit/system reliability
  - Need to be fast, flexible, minimally intrusive
- Software-Implemented Fault Tolerance:
  - Suitable to implement low-cost fault tolerant applications on commercial hardware.

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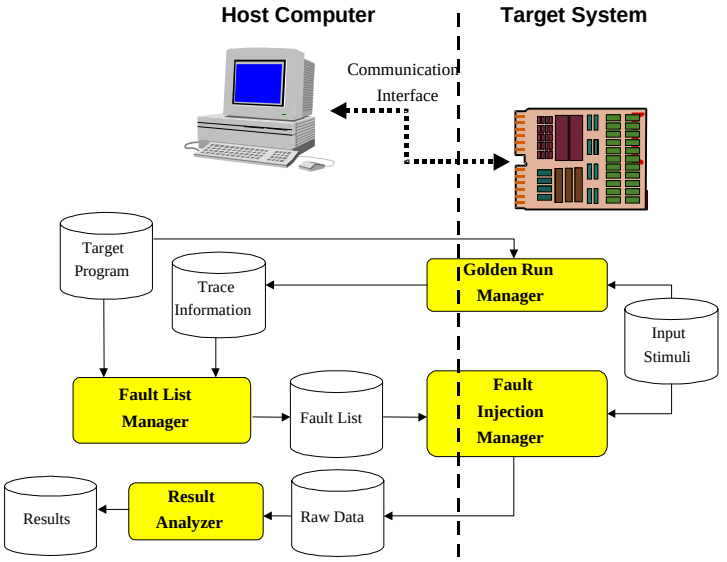
Fault Injection Environment



Fault Injection Techniques

- ***Simulation-based***
- ***software-based***: **instruction execution is monitored by forcing the µP into Trace Mode**
- **based on *Background Diagnostic Mode* (BDM), available in some Motorola processors**
- ***hardware-based***: **a low-cost, programmable board for speeding-up and supporting the Fault Injection experiments**
- ***FPGA-based***: **an FPGA board is exploited to emulate the good and faulty circuits (for circuits and µP systems).**

TODAES99

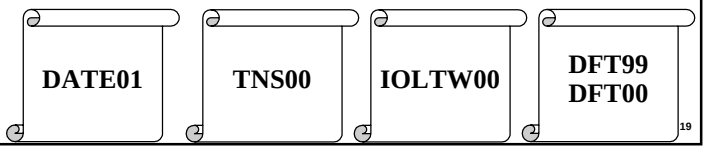
VTS99

SAFE COMP00

IOLT01

Software Fault-Tolerance

- **Rules for automatically transforming high-level code in order to obtain safety:**
  - **To detect faults in the data:**
    - **duplicate every variable**
    - **check for consistency after every read access**
  - **To detect faults in the code:**
    - **repeat any operation**
    - **check for control flow consistency.**
- **Experimental validation via Fault Injection and Irradiation.**



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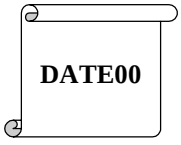
Fault Injection in a Co-Design Framework

- **It allows to early select the architecture that best fits the design constraints and to evaluate its dependability**
- **Fault Injection at a behavioral and structural level**
- **Faults are injected both in the h/w and s/w parts.**



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For more information

At *`http://www.cad.polito.it/`* you can find:

- **bio info**
- **papers**
- **tools and benchmarks**
- **contact info.**