COTEST - Current Status

Zebo Peng
Embedded Systems Lab (ESLAB)
Linköping University

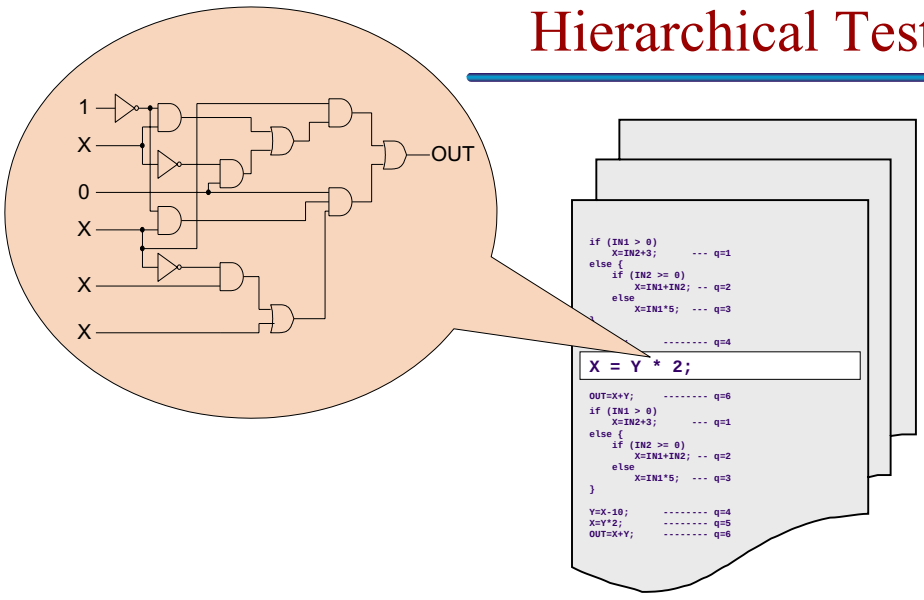
Recent Activities at LiU

- Hierarchical test generation
  - Implementation using a constraint solver (Prolog)
  - Extension to behavioral level descriptions
  - Experimental work to demonstrate the efficiency of the proposed approach
- Insertion of testability into high-level design: Hybrid BIST

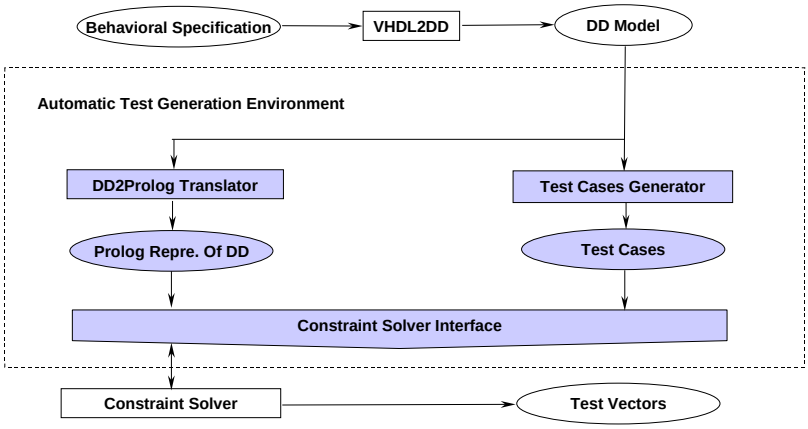
Hierarchical Test at Behavioral Level

- Using structural information in behavioral level test generation
- Use behavioral level for propagation and justification while tests for functional units are generated based on gate level representation
- An approach for early design space exploration to evaluate testability
- Fault coverage is measured on a structural level against stuck-at faults

Hierarchical Test



Automatic BTG Environment



Testing of behavior

- Introduction of control states into the specification
- Conversion of modified specification to DDs
- Test generation based on code coverage metrics

Testing FU-s

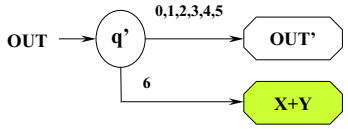
- Library of FU-s
  - VHDL models on a behavioral/structural level
  - DD models on a structural level
- PODEM algorithm for gate-level test generation
  - With "intelligent" method to handle X values and constants
- Justification and propagation on a behavioral level

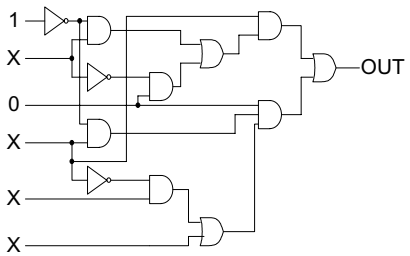
Testing FUs

```
if (IN1 > 0)
    X=IN2+3;        --- q=1
else {
    if (IN2 >= 0)
        X=IN1+IN2; -- q=2
    else
        X=IN1*5;   --- q=3
}

Y=X-10;         -------- q=4
X=Y*2;          -------- q=5
OUT=X+Y;        -------- q=6
```

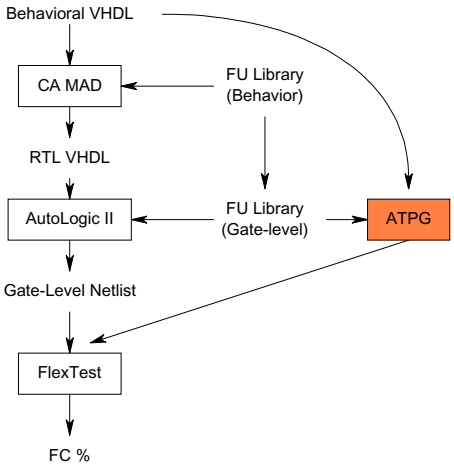
Behavioral Description





Gate-level netlist

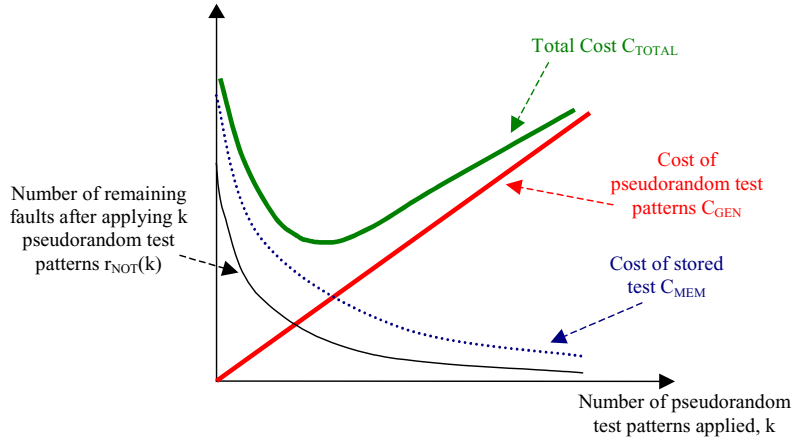
Experimental Environment



Insertion of Hybrid BIST

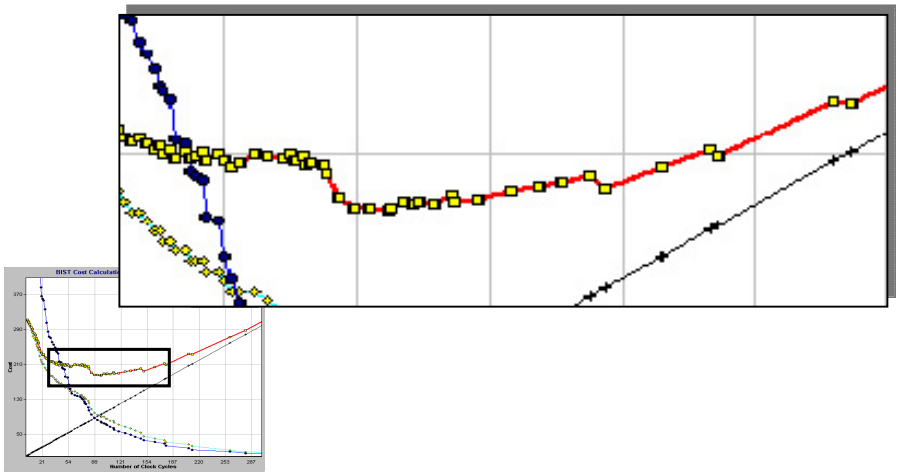
- Our objective:
  - Insertion of hybrid BIST structure into a design to improve its testability.
  - Optimal balance between pseudorandom and deterministic test patterns in terms of time and memory without losing fault coverage
  - To implement the test architecture in software to avoid area overhead, not to affect system performance and to provide possibility for test reconfiguration

Cost Calculation for Hybrid BIST

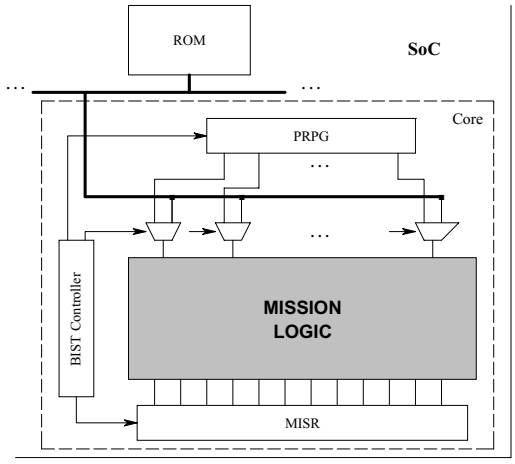


$$C_{TOTAL} = \alpha L + \beta S = C_{GEN} + C_{MEM}$$

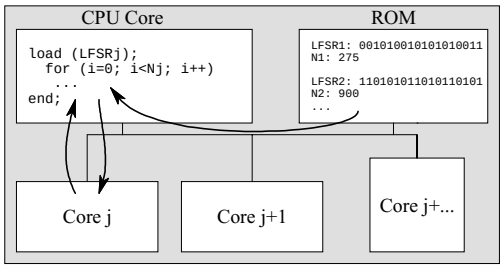
Cost Calculation for Hybrid BIST



Hardware Based Hybrid BIST Architecture

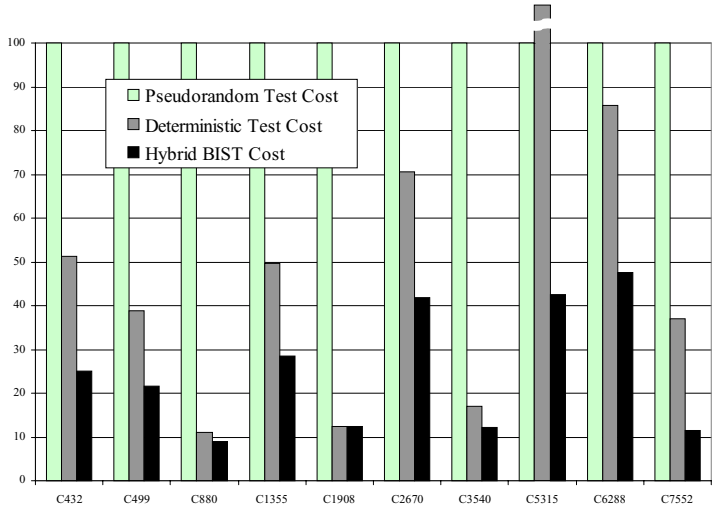


LFSR Emulation



- One test program for all cores
- LFSR characteristics stored in the ROM
- Test program executed in the process core
- Signature analysis and compaction also by the software
- No HW constraints

Experimental Results



Future Plan

- Fine tuning based on experiments with the hierarchical test generation technique.
- Integration of the two techniques together.
- Demonstration with the benchmark examples identified in the first step of COTEST.