**Ying Zhang**

Email: [ying.zhang@liu.se](mailto:ying.zhang@liu.se) Phone: 046-0727156188 Date of Birth: 1984.3.4

Address: Rydsvägen 210A LGH 1101, Linköping, Sweden

**EDUCATION**

2011.9~present **Computer Science, Embedded System Lab, Linköping University, POSTDOC.**

Supervisor: **Zebo Peng,** Director of ESLAB, IDA, Linköping University

2006.9~2011.7 **Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, PH.D.**

Ph.D. supervisor: **Huawei Li,** Professor of Institute of Computing Technology

Honor: 2010 XiaPeisu Scholarship

2008 CAS Merit Student

2002.9~2006.7 **Computer Science and Technology, Haerbin Engineering University, Haerbin, Heilongjiang Province, Bachelor Degree**

Honor: 2006 Outstanding Graduates of Heilongjiang Province

2002~2006 Haerbin University Merit Student

**RESEARCH EXPERIENCES**

2011.9 – present: **High-level Automatic Test Program Generation for Superscalar Processors**

Motivation: It is the first time to test superscalar and out-of-order processors with software-based self-testing method

Contribution: Apply Bounded Model Checker to excite all function paths of the superscalar processor and automatically generating test programs.

2009.12 – 2011.9: **Software-Based Self-Test (SBST) for Processors** (Chinese National Natural Science Funds, 2005)

Motivation: SBST enables the processors to test themselves and other circuits.

Contribution: Present a method for automatic test instruction generation (ATIG) on ATS’2010.

Present a test program generation method for hidden control logic in pipeline processors on TVLSI. (Under Review)

2007.6 – 2010.2: **Fault-Tolerant Design for Crosstalk effects on Interconnects** (Chinese National Natural Science Funds)

Motivation: Apply fault-tolerant design to avoid or tolerate the large delay induced by crosstalk effects.

Contribution: Propose selected crosstalk avoidance code (SCAC) to avoid crosstalk-induced delay through forbidding certain signal transition and publish this work on VTS’2008.

Design a reliable NOC router with SCAC, and present it on ATS’2008 & JCST’2009.

Design selected signal transition time adjustment method to tolerate crosstalk effect on NOC interconnects on TVLSI’2011.

**PUBLICATIONS**

* **Ying Zhang**, Huawei Li, Yinghua Min, Xiaowei Li “Selected Transition Time Adjustment for Tolerating Crosstalk Effects on Network-on-chip Interconnects”, IEEE transactions on VLSI systems, Vol.19, 2011, pp.1787-1800.
* **Ying Zhang**, Huawei Li, Xiaowei Li, “Selected crosstalk avoidance code for reliable network-on-chip”, Jounal of computer science and technology 24(6): 1074–1085 Nov. 2009.
* **Ying Zhang**, Huawei Li, Xiaowei Li, Yu Hu, “Codeword Selection for Crosstalk Avoidance and Error Correction on Interconnects”, in proceeding of IEEE VLSI Test Symposium 2008, pp.377-382.
* **Ying Zhang**, Huawei Li, Xiaowei Li, “Reliable Network-on-Chip Router for Crosstalk and Soft Error Tolerance”, in proceeding of IEEE Asian Test Symposium 2008, pp.438-443.
* **Ying Zhang**, Huawei Li, Xiaowei Li, “Software-Based Self-Testing of Processors Using Expanded Instructions”, in proceeding of IEEE Asian Test Symposium 2010, pp.415-420.
* **Ying Zhang**, Huawei Li，Xiaowei Li，" MT Compacted Set for Interconnect Crosstalk on SoC"，Journal of Computer-Aided Design & Computer Graphphics 2009, pp.476-480.
* **Ying Zhang**, Huawei Li, Xiaowei Li, "MT Comtacted Set for Interconnect Crosstalk on SOC", Digest of Papers, IEEE 8th Workshop on RTL and High-Level Testing (WRTLT'07), October 12-13, Beijing, pp.125-130.
* **Ying Zhang**, Huawei Li, Xiaowei Li, “Automatic Test Program Generation Using Executing Trace Based Constraint Extraction for Embedded Processor”，TVLSI’2011.(Under Review)

**PATENT**

* Ying Zhang, Huawei Li, Xiaowei Li, “a design method and system for reliable interconnects on chip", the number of copyright:100592308.
* Ying Zhang, Huawei Li, Xiaowei Li, “a reliable network-on-chip router", the number of application: 200810117249.5.