Strategic Integrated Electronic Systems Research (STRINGENT)

0. Summary.

We propose a strategic research program, STRINGENT, aiming at basic research in integrated electronic systems. The proposal is based on a broad and well-proven competence at four groups at Linköping University. Overall goals are to find new methods considerably improving our ability to convert a loosely specified idea into silicon, to improve power and cost efficiency of embedded electronic systems, and to find methods to considerably reduce the development time for an embedded electronic product. We present a research plan, including specific research projects aiming at these goals. The proposed projects are converging into a few common demonstrators, thus integrating the various subtopics. We describe how STRINGENT will interact with undergraduate education, applied research programs and industry, facilitating an effective dissemination of results. A 5 year program is proposed, with a total budget of 150MSEK (15MUSD), of which 75MSEK is applied for in this application.

1. Background.

The unprecedented development of integrated electronics since the sixties is the main factor behind the IT society of today. The pace of development is expected to continue for many years to come. In order to keep the strong position in this area in Sweden, it is essential to continue with high quality research and education in the field. In this context, we must establish a good direction for our development of the knowledge. After seeing the development of semiconductors, integrated circuits, fabrication techniques, processors, memories and digital signal processing, we now expect the development of highly integrated, very compact complex systems with broad application areas. The real challenge is to master the complexity of these systems, utilizing all previous accumulated knowledge. Important application areas are communication, media and control, often termed embedded electronic systems. Key future expectations of these systems are complex functionality, high reliability and security, very low power consumption and volume, and low cost. New application directions may be ultra low power systems for the everyday small commodities, or very high performance systems for phased array antennas for better utilization of the frequency spectrum or for image-forming radars.

Linköping University aims for essential contributions to these fields. This will be accomplished through three connected actions, an education program, an industrial research program and a long-term basic research program, conducted by Centrum för Elektronik at LiU. The educational program has been initiated, in the form of a profile of Y- and D-programs in Linköping, combined with an international master program, the Socware educational program. The industrial research program is under development in cooperation with Acreo, KTH and LTH, under the name of Socware (partly financed directly via The Ministry of Industry, Employment and Communications). The basic research program, finally, is the topic for this application.

Linköping University is very well prepared for this program. We have historically built a very strong activity in this field, through basic research financed by STU, NUTEK, TFR and SSF. A strong base of experienced researchers has been built; we are now 6 professors and 6 associate professors in place and we have one more professor under recruitment. Presently, we have a large and successful basic research activity, financed mainly by the SSF research schools Intelect and to some extent Ecsel (The Intelect program was originally designed by Christer Svensson). Through Intelect we have 17 ongoing graduate student projects (more than 1/3 of the national research school), and through Ecsel 2 projects. Finally we have a powerful suite of software to support our research, run on modern Unix- and Windows-based workstations, and well-equipped laboratories for experimental verification of fabricated chips.

2. Scientific vision and main goals

The proposed basic research program: "Strategic Integrated Electronic Systems Research" aims at developing the next generation knowledge, to be the basis for future education and industrial research. We have identified three key areas of research, *System design, Technology utilization and Design efficiency*. *System design* aims for new methods to manage the complex task of taking an application idea through the specification of an electronic system to a suitable SW-HW architecture and implementation in silicon. *Technology utilization* aims for the ability to fully utilize available technology for maximum performance at minimum power, volume and cost. *Design efficiency* aims for the ability to design a complete, verified and testable product in very short time. Each of these areas contains real challenges beyond the knowledge of today.

Our vision is to make our competence, circuit and system sciences, lead the development of future electronics, instead of as previously materials, processes and devices.

Our aim is to maintain and further develop our national and international recognition for excellence in integrated electronic systems research, through basic research in System design, Technology utilization and Design efficiency.

Overall goals are to find new methods considerably improving our ability to convert a loosely specified idea into silicon (*System design*), to improve power and cost efficiency of embedded electronic systems (*Technology utilization*), and to find methods to considerably reduce the development time for an embedded electronic product (*Design efficiency*).

Our educational goal is to produce 3-4 Ph.D. per year and a similar number of licentiates.

3. Relation to other programs

As mentioned in the introduction, STRINGENT aims at basic research and graduate education. The STRINGENT program can be further strengthened by projects financed by for example the Swedish Research Council (VR). As a complement, we perform undergraduate education and industry related research, both supported by the Socware program, in cooperation with Acreo and other Swedish universities. We have chosen to

treat the basic research separated from our applied research in this application, but certainly the two activities benefit considerably from each other.

4. Research plan

The research plan is partitioned into 3 work packages, *System design, Technology utilization and Design efficiency,* all aiming at the same goals. We describe these work packages below, with a few concrete research projects in each package.

4.1. Work package: *System Design.*

4.1.1 Research Area

The functionality implemented in current communication systems, e.g., high-speed modems, is indeed very large and is expected to continue and increase rapidly. Current design methodologies, HW architectures, and tools are rapidly becoming antiquated and make the design and implementation of each new generation of systems more and more difficult and risky. Even more disturbing is that new problems occur due to a widening gap between knowledge, methods, terminology, traditions, etc. used by designers working on different aspects of the design, e.g., the application, system, and electronics domains. System designs tend to become complex when more aspects have to be considered besides the basic function, e.g., flexibility, reuse, development time, and power consumption. These problems are also aggravated by the trend of reduced time between new research results, market identification, and their industrial application.

4.1.2 General Approach

We aim at alleviate or reduce the problems with increasing system complexity and design effort by developing more efficient design procedures and tools and bridging the gap between different knowledge domains. This will be achieved by developing design strategies and modeling techniques as well as educating people that are able to transcend many, if not all levels of abstraction involved the design process. We believe that this work needs to a large extent be domain-specific. In our case telecommunication and signal processing are the main areas of application.

Besides problems stemming from the increasing system complexity the major design tradeoffs are between *flexibility*, *energy efficiency*, and *design effort*. Flexibility in this context involves issues like ease of reuse (IP), modification (redesign/programmable), while energy efficiency and design effort usually are not compatible with large flexibility.

To reduce the design effort and obtain a good overall implementation we propose the following approach. Using an essentially top-down approach a complete specification and system model is developed through a sequence of models with increasing degrees of functionality (completeness). We refer to this as the *problem-understanding phase*. This phase, which is very important, is usually not included in the system design and implementation phases, which may lead to poor designs. We therefore aim to integrate the problem-understanding phase with the system and implementation phases to arrive at a vertical design process without major bottlenecks and avoid handovers between different categories of designers. A key word here is *vertical integration*.

Once the system specification and its executable high-level models are finalized they can be partitioned into suitable subsystems that can be derived in a similar fashion. This process can continue recursively, were subsystem models described using high-level algorithmic models are gradually synthesized using more elementary algorithms or components, allows verification/validation to be made between the different abstraction levels. This approach also support design space exploration and optimization at each level of abstraction. We believe that this is an efficient way to significantly increase the design efficiency and ascertain a correct and efficient implementation. This approach is also compatible with a meet-in-the-middle approach that is suitable for IP reuse.

To reduce the design effort and better support the overall optimization as well as simplify the mapping to a software/hardware structure we advocate a domain-specific approach that focuses on internal communication between different subsystems and components. This is due to the fact that most components (software/hardware blocks) in telecommunication and signal processing applications are interconnected and operate as a data-flow system.

Efficient SW/HW components are also needed as well as a general hardware structure suitable for deep sub-micron CMOS processes. We will in this area develop a matching GALS–Globally Asynchronous, Locally Synchronous architecture, with corresponding communication circuitry and design tools. The GALS approach has many potential advantages: reduces energy consumption, avoids clock problems, support reuse of IP blocks and reduces the design effort. Of course, development of flexible and energy efficient IP blocks is another important topic where the algorithm-arithmetic-hardware structure needs to be co-optimized.

4.1.3. Research Projects

4.1.3.1. Filter bank based multi-carrier systems

Multi-carrier systems are used both for wired (e.g., ADSL and VDSL) and wireless systems (e.g., IEEE 802.11a and HiperLAN) to obtain high data rates in difficult transmission environments. Current multi-carrier systems utilize computational efficient FFT (Fast Fourier Transform) based filter banks (FBs) which, however, have several drawbacks. The use of more sophisticated multirate FBs can provide improved robustness, simplified synchronization and equalization, reduced transmitted power for a given bit error rate, and reduced power consumption [1].

One main line of work will be on near-perfect reconstruction (PR) FBs which, instead of the more traditional PR FBs, should be used in order to minimize the power consumption. Another line is on asymmetric FBs for communication systems consisting of a stationary and a mobile unit. Such asymmetric FBs have been proposed recently, but only for use in filter bank based analog-to-digital converters [2].

[1] P. P. Vaidyanathan, “Filter banks in digital comm.,” IEEE Cir. Sys. Magazine no. 2, 2001.
[2] P. Löwenborg, H. Johansson, and L. Wanhammar, “A survey of filter bank A/D converters,” Proc. Swedish SOC Conf., Arild, Sweden, Mar. 20–21, 2001.

4.1.3.2. Efficient design of wireless communication platforms

The communication and interconnect based strategy is as essential for both our system design approach and SW/HW structure and we propose to develop a complete design flow from a high-level system model down to an implementation using a communication-

based hierarchy of models that aim at reducing the design effort and supports an implementation using a heterogeneous, Globally Asynchronous, Locally Synchronous (GALS), software/hardware structure. The project will focus on implementation of the digital platforms for PAN (Personal Area Networks), but the RF parts are not included. We plan to get access to the RF components by cooperating with research project 4.2.3.1.

[3] T. Njølstad, O. Tjore, K. Svarstad, L. Lundheim, T.O. VedaI, J. Typpo, T. Ramstad, L. Wanhammar, E.J. Aas, H. Danielsen, "A socket interface for GALS using locally dynamic voltage scaling for rate-adaptive energy saving," Proc. 14th Annual IEEE Intern. ASIC/SOC Conf., Rochester, 2001, pp. 110 - 116.

4.1.3.3 Network-based bus system for system-on-chip integration

There are two challenges while integrating HW/SW IP into a SoC, the design of communications between IPs, and the long verification time. No good SoC integration method can solve the two problems mentioned above. The current way of SoC integration is the custom functional design connecting IP hardware and software ports.

We will develop a Synthesizer and its flow to generate our SoC BUS IP as IP interface. The synthesizer can generate the hardware ports, the network, and software driver towards the operating system. At the same time, we will utilize the full capability of a given silicon technology to maximize the communication capacity.

[4]. D Wiklund and D Liu, Switched interconnect for system-on-a-chip designs, IP2000, UK

[5]. W. J. Dally and B. Towles, Route packets, not wires: On-chip interconnection networks, Proceedings of the Design Automation Conference (DAC), 2001

4.1.3.4. Application Specific Instruction Set Processors (ASIP)

Complete vertical partition is identified as an important route to more efficient design and verification and will lead to systems based on localized processes and storage. In cases when complete vertical partition is feasible, a large machine will be replaced by a set of small processors, here called application specific instruction set processors (ASIPs). We intend to investigate two such systems. We propose to continue our research on protocol processors, which is one kind of ASIP. Speed- and power-efficient architectures and hardware and software development environment for protocol processors will be demonstrated. We will also continue our low power scalable DSP processor research. A basic platform has been defined and we plan on developing an ultra low power audio decoder application.

[6]. Tomas Henriksson, Hardware architecture for protocol processing, LIU-TEK-LIC-2001.48

[7]. T. Glökler, H Meyr, Power reduction for ASIPS: A case study, 2001 IEEE Workshop on signal processing systems.

4.1.4. Milestones

Projects	Modeling (Year1)	Optimization (Year3)	Design & Implement.(Year5)
4.1.3.1	Modeling simulation OFDM system with FB	Performance requirements on FB from system specification	Filter banks used in OFDM systems
4.1.3.2	Multi-point-to-multi-point asynchronous channels	Performance estimation for GALS based systems	Demonstrator SW/HW of GALS based OFDM system
4.1.3.3	Behavior of routing and algorithms	SW/HW application interface optimization	Implementation of SoC BUS HW/SW (port protocols)
4.1.3.4	Protocol processor architecture model	Code optimization and generation	Protocol processor demonstrator

4.2 Work package: *Technology utilization.*

4.2.1. Research area.

The objective of our proposed research is to learn how to utilize the underlying technology to its limits. These limits are of course moving as technology scales, but we aim at solutions that are scalable with the technology development. We expect the underlying technology to be mainstream digital CMOS technology, available through major chip vendors. In 5 years we expect that such a strategy will facilitate a power efficiency of the order of 1000 MIPS/mW (from 1-10 MIPS/mW today) and a chip capacity of 1,000,000 MIPS per chip (from 10,000 today).

We foresee several challenging problems needed to be solved. Examples of such issues are poor scalability of interconnects and managing on-chip communication, increased on-chip noise and managing sensitive circuits in noisy environment, decreased supply voltage, increased parameter spread and integration of sensitive analog circuits.

4.2.2. General approach.

We will utilize a number of different strategies to reach our goals.

We aim at deepening the understanding of the basic technology limits, such as basic physical limits to computation and communication, properties of devices and interconnects in future technologies, effects of noise, and limitations related to packaging and circuit boards.

We aim to understand the communication processes in large systems on chip, enabling the development of new system architectures and design principles based of this knowledge. Such new principles probably include global asynchronous local synchronous approaches (GALS), very high data rate per wire (as well inside a chip as between chips), open, scalable and configurable heterogeneous multiprocessor principles, and distribution of memory among the computing resources.

We aim to develop of the interface to the surrounding world, wire, wireless or fiber communication links, sensors and actuators, in the direction of more generic and efficient solutions to the interface problems.

We aim at demonstrating all results through experimental implementation in Silicon.

4.2.3 Research projects.

4.2.3.1 Generic RF front-end.

We aim at developing very wideband, generic RF front-ends, facilitating software radio or software sensor. The idea is to replace existing front-ends with a wide-band LNA and AD converter combination with enough performance to compete with existing high performance (in terms of sensitivity and selectivity) radio receivers. Such systems have been developed for special purposes, e.g. for GPS receivers [1]. N-MOS transistors are particularly suitable for high-speed sampling and preliminary investigations of RF samplers indicate that reasonable high demands can be met for a carrier frequency of 2GHz [2]. Possible new methods facilitating this development are limited analog preprocessing, digitally controlled tuning of the analog parts and digital adaptive compensation of the analog errors.

[1] Brown and B. Wolt, “Digital L-band Receiver Architecture with Direct RF Sampling”, IEEE Position Location and Navigation Symposium, p. 209, 1994.

[2] D. Jakonis, K. Folkesson and C. Svensson, “RF Sampling Receiver”, Proc. Swedish System-on-Chip Conference 2002, March 18-19, 2002.

4.2.3.2 Global on-chip communication.

Global on-chip communication is today severely limited by wire RC-delays and power consumption [3]. We intend to overcome this limit by utilizing microwave principles applied on upper-metal wires. We propose to utilize very high data-rate signals at low power levels run on microstrips for global chip communication. It has been shown that such wires can carry up to 100Gb/s data-rates. This calls for careful analysis and design of the microstrips, for the development of appropriate drivers, and for the development of appropriate receivers that include retiming and equalization. Preliminary investigations show that high data-rates, low latency and low power consumption can be combined [4]. We expect to have data-rates of 100Gb/s at latencies of the order of speed of light delay over relatively narrow buses. This project is closely related to the network-based bus system discussed under Work package System design.

[3] D. Sylvester and K. Keutzer, "Impact of Small Process Geometries on Microarchitectures in Systems on a Chip", Proc. IEEE, Vol. 89, p. 467, 2001.
[4] P. Caputa and C. Svensson, "Low Power, Low Latency Interconnect", Proc. Swedish System-on-Chip Conference 2002, March 18-19, 2002.

4.2.3.3 Off-chip communication.

Recent increase in clock frequencies on-chip is not accompanied by the corresponding increase of external data-rates [5]. We therefore note a growing unbalance between internal computing capacity and external bandwidth on contemporary chips. One way to overcome this limitation is to substantially increase the external data-rates. To some extent we see such a development, through the development of high-speed serial links (e.g. XAUI 10Gbit Ethernet link). We propose to investigate methods to increase external data-rates more generally, for the purpose of chip-to-chip communication on printed circuit boards, and including processor-memory interfaces. We have previously shown that a printed circuit board can carry the frequency. We now propose to develop circuit techniques for the links that facilitates data-rates of 10-20Gb/s per wire and utilizes automatic adaptation to actual electrical properties of the links. Such automatic adaptation includes data retiming [6] and equalization.

[5] B. K. Gilbert, M. J. Degersrom, P. J. Zabinski, T. M. Schaefer, G. J. Fokken, B. A. Randall, D. J. Schwab, E. S. Daniel and S. C. Sommerfeldt, "Emerging Multigigahertz Digital and Mixed-Signal Integrated Circuits Targeted for Military Applications: Dependence on Advanced Electronic Packaging to Achieve Full Performance", ", Proc. IEEE, Vol. 89, p. 426, 2001.
[6] F. Mu and C. Svensson, "Self-tested self-synchronization circuit for mesochronous clocking", IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 48, p.129, 2001.

4.2.4. Milestones

Projects	Year1	Year2	Year3	Year5
4.2.3.1	Prestudy of sampler and	Sampler test-chips evaluated	Digital algorithms for tuning and error corr.	See 5
4.2.3.2	Prestudy of long distance interconn.	Test design of 50Gb/s bus	50Gb/s bus experim. verified	See 5
4.2.3.3	Definition of demonstrator	Design of tranceiver for 10Gb/s I/O	Test chip tranceiver and equalizer	Very high bandwidth bus demonstrated

4.3. Work package: *Design efficiency.*

4.3.1. Research Area.

The objective is to develop methodologies and tools for the design of complex electronic systems, with design efficiency as the main focus. Modern electronic systems are usually

characterized by sophisticated functionality and consist of a large number of components implemented in hardware (both analog and digital) and software. Very often there are strong interactions with the environment and demanding requirements in terms of performance, power consumption, cost, size, weight, etc. This research will concentrate on the early design phases (system level design), including specification, modelling, partitioning, architecture selection, communication synthesis, verification and design for test. The expected results will contribute to the improvement of cost, efficiency and reliability of the final electronic products as well as improvement in design productivity.

One of the main cornerstones of our research is the fact that, due to increasing complexity, the design process has to move towards a methodology in which relatively complex blocks are combined in order to deliver the required functionality (instead of designing from scratch). With such a design process, the focus is on the interaction of components and, in particular, on interfaces, protocols and glue logic which interconnect independent components allowing them to behave in a coherent way and to perform the required functionality.

The systems we are targeting are complex embedded systems with strong requirements regarding the delivered quality of service and safety. Thus, the following aspects are of particular interest:
- design reuse (as the only way to manage complexity of designs)
- analysis and performance estimation (to guarantee QOS)
- verification (to guarantee certain properties the models)
- testing (to verify the correctness of the manufactured SOC).

4.3.2. General Approach.

Our main approach is to develop techniques to allow designers to explore a set of design alternatives for SoC designs. In particular, we will develop a methodology to facilitate the reuse of IP components as part of the new architecture in the context of SoC design for telecommunication applications.

We believe that a transformational design approach in which partitioning and architecture selection steps are performed iteratively and are guided automatically by an optimization heuristic strategy and/or by user interaction is a way to handle the complexity of such a design process. It is very important to provide an environment in which the experience and skills of the individual designer are combined with the power of design automation tools in order to identify the proper architecture for a given application. Thus, several elements of the architecture could be fixed by the designer, narrowing the design space. An alternative strategy is to let the design tool identify, based on certain heuristics, areas of the design space, which should be further explored and analysed by the designer.

The problem becomes extremely interesting in the context in which several, contradicting tradeoffs have to be considered, especially for applications in which low energy consumption is essential. The designer has to reach the right balance between, for example, flexibility and power consumption by deciding how certain parts of the functionality are implemented in hardware or software. Similar decisions have to be taken concerning the use of application specific or respectively general purpose processors. In order to find the right balance, a new generation of design environments is needed incorporating specification, estimation, simulation, and optimisation tools.

Design space exploration has to be supported by complementary tools for simulation and performance modelling and formal methods. In this context, we are particularly interested in two aspects: stochastic modelling and analysis, and the combination of simulation and formal verification. Certain properties of the system, like safety critical aspects, have to be formally checked. A particularly interesting aspect is how to integrate formal verification techniques into a component-based design process.

The design of complex SOCs has generated new challenges regarding the testing of manufactured chips. The only solution to this challenge is the elaboration of advanced design for test techniques. For the coming generation of complex electronic systems testing techniques have to take into consideration the fact that large parts of the functionality will be implemented as software. Another interesting aspect is the interplay between behavioural level verification and testing of production faults.

4.3.3. Research Projects.

4.3.3.1 System Modelling.

System modelling is of outstanding importance for handling the increasing complexity of the design process. It has a strong impact on the main system synthesis tasks, like performance estimation, verification and design space exploration. Several aspects have to be taken into consideration, in this context:

- Expressive power needed in order to capture the relevant properties of the target systems.
- Support for a transformational design process.
- Suitability for both simulation and formal reasoning.
- Integration into a communication-based design concept with component reuse.

One alternative could be a Petri-net based representation with extensions concerning timing and dataflow, as well as hierarchy. The representation should support both deterministic as well as stochastic modeling.

[1] L. A. Cortes, P. Eles and Z. Peng, Hierarchical Modeling and Verification of Embedded Systems, Proc. Euromicro Symposium on Digital Systems Design (DSD), Warsaw, Poland, September 4-6, 2001, pp.63-70.

[2] L. Lavagno, A. Sangiovanni-Vincentelli, E. Sentovich, Models of Computation for Embedded System Design , Ahmed A. Jerraya and Jean Mermet eds.: System Level Syn-thesis, Kluwer 1999.

4.3.3.2 Simulation and Performance Analysis.

During successive design phases both correct functionality and performance of a certain design alternative have to be checked. Both simulation based techniques, and analytical approaches should be supported.

In the context of performance estimation, we find it extremely important to also support stochastic modelling and analysis. Current approaches to analysis of time-constrained systems are based on worst-case assumptions, in particular, worst-case execution times. This leads to over-designed systems with high cost and power consumption in situations in which an much cheaper implementation with still delivers the required quality of service could be feasible. An analysis based on probabilistic distribution of execution times can provide extremely useful information on the QOS provided by a certain design alternative and, thus, guide the design space exploration towards cost and power-effective implementations.

[3] S. Manolache, P. Eles and Z. Peng, Memory and Time-Efficient Schedulability Analysis of Task Sets with Stochastic Execution Time, Proc. 13th Euromicro Conference on Real-Time Systems, Delft, the Netherlands, June 13-15, 2001, pp.19-26.
[4] A. Colin, I. Puaut, Worst Case Execution Time Analysis for a Processor with Branch Predic-tion , Real-Time Systems, V18, N2/3, 2000.

4.3.3.3 Formal verification for component-based designs.

The specification approach, as presented above, allows for the specification of executable models. These models can be simulated in the context of different resources and mappings of functionality to these resources. However, such a simulation-based approach, although useful for functional verification and design space exploration, has to be complemented by a support for formal verification. Certain properties of the system, like safety critical aspects, have to be formally checked. We see a very good link from the initial specification through the Petri-net based design representation, to model checking tools. In particular, we are interested in component-based designs and checking properties related to timing constraints. A problem is the lack of information about the internals of pre-designed blocks. This makes an overall verification of the whole system impossible. However, it is reasonable to consider that the design of each individual component has been verified before delivery and can be supposed to be correct. What remains to be verified is the correctness of the interface logic (hardware or software) and the way components interact. Such an approach can handle both the complexity aspects (by a design and conquer strategy) and the lack of information concerning the internals of predefined components.

We propose a systematic synthesis flow and a verification methodology based on a formal representation using Petri nets, as mentioned above. One of the basic ideas is to associate to each predefined library component a set of predicates, expressing input/output constraints. Such predicates should be delivered together with the component. The goal is to verify the correctness of the new system (in terms of functionality and timing), based on the predicates associated to reusable components and the Petri-net based model corresponding to the interface logic produced by the designer.

[5] L. A. Cortes, P. Eles and Z. Peng, Verification of Embedded Systems using a Petri Net based Representation, Proc. 13th International Symposium on System Synthesis (ISSS 2000), Madrid, Spain, Sept. 20-22, 2000, pp. 149-155.
[6] K. Keutzer, et al. System level Design: Orthogonalization of Concerns and Platform-Based Design , IEEE Transactions on CAD, V19, N12, 2000.

4.3.3.4 Testing and Design for Test.

Testing of complex SoCs is one of the most critical aspects of the SoC technology. In this context we plan to work in the two directions. The first one deals with the development of build-in self-test (BIST) techniques for system-on-chip designs. In particular, we will develop techniques to optimize BIST resources usage and to enhance testability during the synthesis process. We will also address hybrid BIST technique, where pseudo-random test pattern based self-test is combined with deterministic test patterns.

In the second direction, we will investigate design for testability techniques in which both hardware testability and testability of the software components are considered in order to improve the global testability of the system. The final aim will be to develop a design environment for hardware/software codesign where testability is considered as design criteria the same way as performance, cost and power consumption.

[7] E. Larsson, and Z. Peng, An Integrated Framework for the Design and Optimization of SOC Test Solutions, Journal of Electronic Testing; Theory and Applications (JETTA), Vol. 8, No. 4, August 2002.
[8] Y. Zorian, Emerging trends in VLSI test and diagnosis, Proceedings IEEE Workshop on VLSI, 2000, pp.21-27.

4.2.4. Milestones

Projects	Year1	Year2	Year3	Year5
4.3.3.1	Petri net based design model	Final Petri-net model		Integration into a holistic component-based design, verification, and test methodology Case studies using industrial examples to demonstrate the efficiency of the proposed techniques
4.3.3.2	.	Platform based on Petri-net		
4.3.3.3	Component-based approach formulated	Component-based Petri-net model Stochastic methods for performance analysis	Component-based verification methods Stochastic-based performance tool implemented	
4.3.3.4	BIST-based SoC technique sketch		Test methodology with global optimization	

5. Milestones.

Detailed milestones for the research projects are given in connection the project descriptions above. Here we will give milestones covering all work packages.

Projects	Year3	Year4	Year5
4.1.3.3 4.2.3.2	Network-based bus integrated	Test-chips designed	Test-chis evaluated
4.1.3.2 4.2.3.1	Flexible RF-receiver system design	Test chips designed	Integration of RF and baseband demonstrated
4.1.3.2 4.3.3.1			Modeling technique demonstrated in wireless platform

6. International standing of the researchers

The applicant and the principal investigators are all internationally well recognized researchers in the forefront of contemporary research and with a good international visibility. For more detailed information, see the curricula vitae.

7. Strategic aspects for Swedish industry

The field of integrated electronic systems is developing at a very high pace since about 30 years, following Moores law. There is no sign of a slowdown of this pace of development. This remarkable pace of development is the main fuel for the fast development of computer, communication and IT industry. It is therefore of uttermost importance for a highly developed country to have a strong basic research activity in this field. This is certainly true also for Sweden, which is heavily dependent on high-tech industry based on electronics. Swedish industry is particularly dependent on system implementation (for telecommunication, sensors and vehicles). Such implementation is

done in software, electronic hardware and mixtures thereof. The field of integrated electronic systems, particularly for embedded systems, is thus a key for Swedish industry.

The proposed basic research program: “Strategic Integrated Electronic Systems Research” aims at developing the next generation knowledge, to be the basis for future education and industrial research related to embedded electronic systems.
Our research has strong links with Swedish and foreign industries, and we expect this contacts to be further strengthened to support the proposed research.

8. Spin-off effects from the centre

As explained in the introduction, STRINGENT is a critical part of a grand plan, including an education program, an industrial research program and a long-term basic research program. The educational program has been initiated, in the form of a profile of Y- and D-programs in Linköping, combined with an international master program, the Socware educational program. The industrial research program is under development in close cooperation with Acreo, under the name of Socware (partly financed directly via The Ministry of Industry, Employment and Communications). Within this program we presently participate in two demonstrators, one multi-band WLAN demonstrator, with several industrial partners and one on-chip network demonstrator, initiated by us. Acreo is chosen as our main channel to industry. This is complemented with direct cooperation with selected companies, for example Ericsson CadLab Research Center, Ericsson Microelectronics and Intel. The basic research program, finally, is the topic for this application. The basic research program includes graduate education.

From the above description we thus conclude that we will have the following spin-off effects:

- Undergraduate education in design of integrated electronic systems.
- Graduate education in the field of integrated electronic systems.
- Competence transfer to industry through Acreo (through consulting, commission and common demonstrators).
- Active support for the establishment of foreign industry in Sweden through Acreo.
- Competence support to selected companies through direct cooperation.
- New companies spinning off University or Acreo (several historical examples).
- Knowledge transfer to Swedish industry through intensive courses.

Historically, we have been very successful at several of the above cases. We have produced 35 doctors in this field during the last 10 years, of which 5 have became professors at various universities. Several companies have spun off our activities recent years, most important Switchcore and Optillion. Acreo has created cooperation with two foreign companies with the goal to have these establish design centers in Sweden. Recent years we have given 2 intensive courses per year to industry.